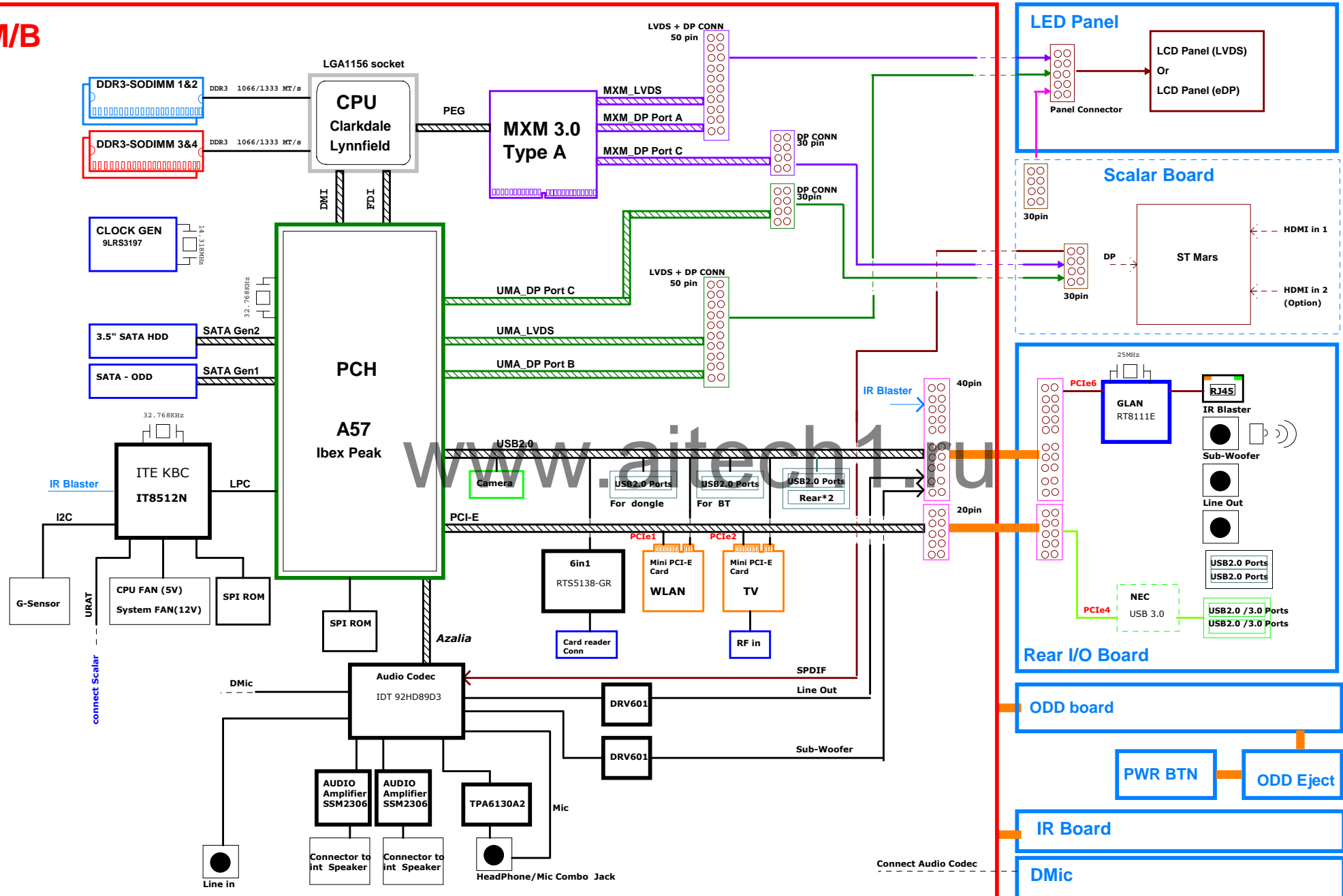


Schematic Page Description :

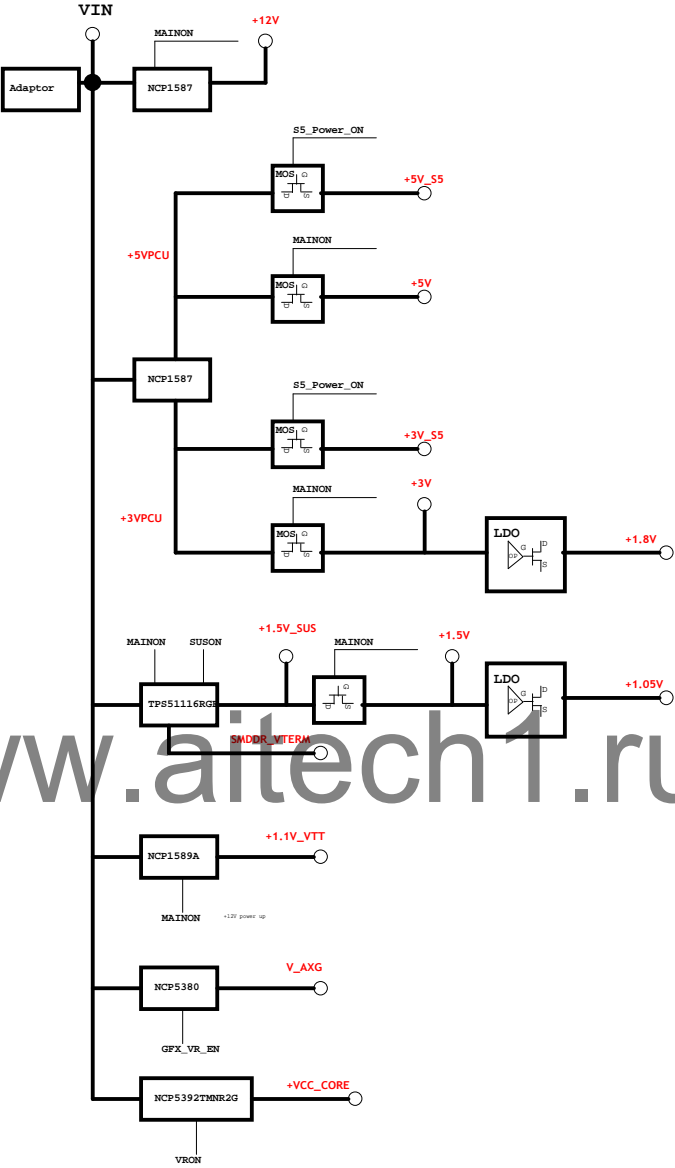
01 -- Page Description	21 -- PCH 1/6 (DMI/FDI/VIDEO)	41 -- FAN/Thermal Protection
02 -- System Block Diagram	22 -- PCH 2/6(SATA/RTC/HDA/LPC)	42 -- ADP AC IN
03 -- Power Map	23 -- PCH 3/6(PCIE/USB/CLK/NV)	43 -- CPU VCC_CORE (NCP5392)
04 -- Power Sequence 1/2	24 -- PCH 4/6(GPIO/CPU)	44 -- VAXG (NCP5380A)
05 -- Power Sequence 2/2	25 -- PCH 5/6(POWER)	45 -- DDR3 1.5V(TPS51116)
06 -- Clock	26 -- PCH 6/6(GND)	46 -- CPU_VTT(NCP1589A)
07 -- SMBus Block Diagram	27 -- MXM 3.0	47 -- +12V/ HDD(NCP1587)
08 -- GPIO list	28 -- Audio Codec(ALC888)	48 -- 3V/5V PCU/S5
09 -- CLOCK GENERATOR	29 -- AMP (MAX9736D)	49 -- +1.8V/+1.05V
10 -- MCP 1/7(CLK/CTRL/MISC)	30-- JMB380 CR &1394	
11 -- MCP 2/7(DDR3 CHANNEL A)	31 -- HDD/ODD	
12 -- MCP 3/7(DDR3 CHANNEL B)	32 -- MINI PCIE (WLAN/TV)	
13 -- MCP 4/7(PCIE/DMI)	33 -- USB/CCD/BT/MT	
14 -- MCP 5/7(VCCP)	34 -- Panel (DP/LVDS)	
15 -- MCP 6/7(MISC/VCC)	35 -- Panel (Control)	
16 -- MCP 7/7(GND)	36 -- CRT	
17 -- SODIMM 1	37 -- EC ITE 8512N/FLASH	
18 -- SODIMM 2	38 -- NVRAM	
19 -- SODIMM 3	39 -- I/O connector	
20 -- SODIMM 4	40 -- XDP/BRAIDWOOD	

F01 System Block Diagram

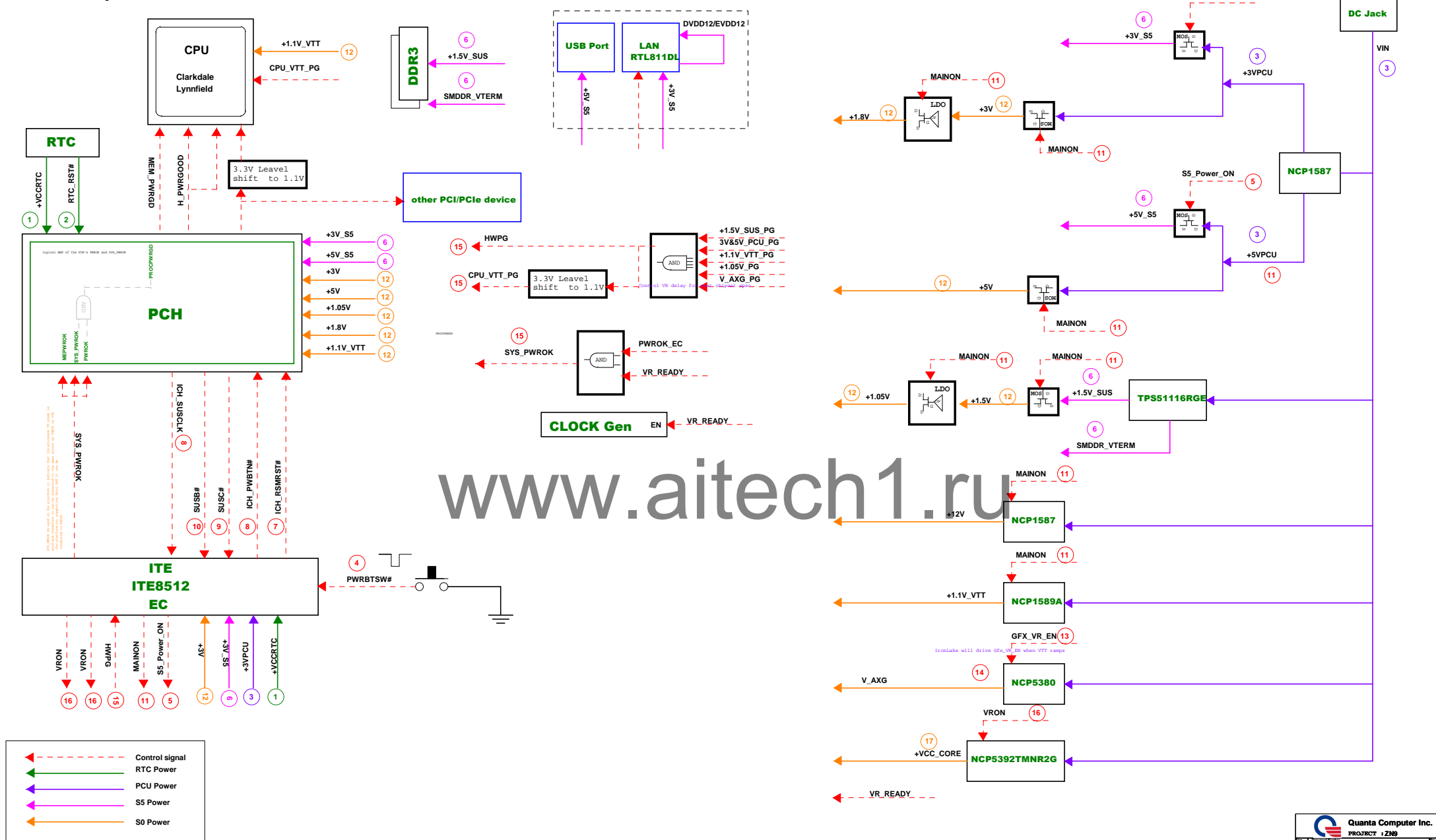
M/B



Power Rail	Destination	Voltage	SO Current
+VCC_CORE	Lynnfield : Default for initial power up	0.65V-1.4V 1.1V	90A(TDC)
V_AXG			
+1.1V_VTT	Lynnfield : Memory controller & shared cache Ibex Peak : DMI_IO	1.045V-1.1V-1.155V 1.1V 1.05V-1.1V-1.16V	30A(TDC) 0.065A 0.001A
+1.8V	Lynnfield : Internal processor PLL Ibex Peak : Internal PLL & VRMs Ibex Peak : Dual channel NAND I/F	1.71V-1.8V-1.89V 1.71V-1.8V-1.89V 1.71V-1.8V-1.89V	1.1A 0.196A 0.156A
+1.5V_SUS	Lynnfield : CPU I/O Voltage for DDRIII DIMM :	1.425V-1.5V-1.575V	6A
SMDDR_VTERM	DDRIII Terminator:	0.75V	2A
+1.05V	Ibex Peak : VccCore Ibex Peak : Vcc core I/O buffer Ibex Peak : DMI buffer voltage Ibex Peak : Display PLL A power Ibex Peak : Display PLL B power	0.998V-1.05V-1.1V 0.998V-1.05V-1.1V 0.998V-1.05V-1.1V 0.998V-1.05V-1.1V 0.998V-1.05V-1.1V	1.629A 3.251A 0.065A 0.075A 0.075A
+1.5V	Mini PCIE : +1.5V(WLAN)		
+3V	Ibex Peak : I/O buffer voltage Ibex Peak : Display DAC Analog power CH7308 : LVDD ALC662 : DVDD Mini PCIE : +3.3V(WLAN) CAREMA	3.14V-3.3V-3.47V 3.14V-3.3V-3.47V	0.357A 0.069A
	Ibex Peak : Core well Ref. voltage SATA ODD SATA HDD(2.5" x SSD) ALC662S : AVDD Touch Screen LCD Panel USB: x 12 ports	4.75V-5V-5.25V 5V	0.001A 6A
+12V			
+3V_S5	Ibex Peak : Intel Management Engine Ibex Peak : Suspend well I/O Buffer Ibex Peak : HD Audio controller Suspend Voltage LAN 82578DM : VDD CLK Gen_CK505 : VDD EC(IT8512) : VSTBY SPI FLASH ROM	3.14V-3.3V-3.47V 3.14V-3.3V-3.47V 3.14V-3.3V-3.47V	0.086A 0.168A 0.006A
+5V_S5	Ibex Peak : Suspend well Ref. Voltage	4.75V-5V-5.25V	0.001A
	INVERTER : Vin FAN_CPU		
+3VPCU			
+5VPCU			
15VPCU			
VIN			



Power Sequence

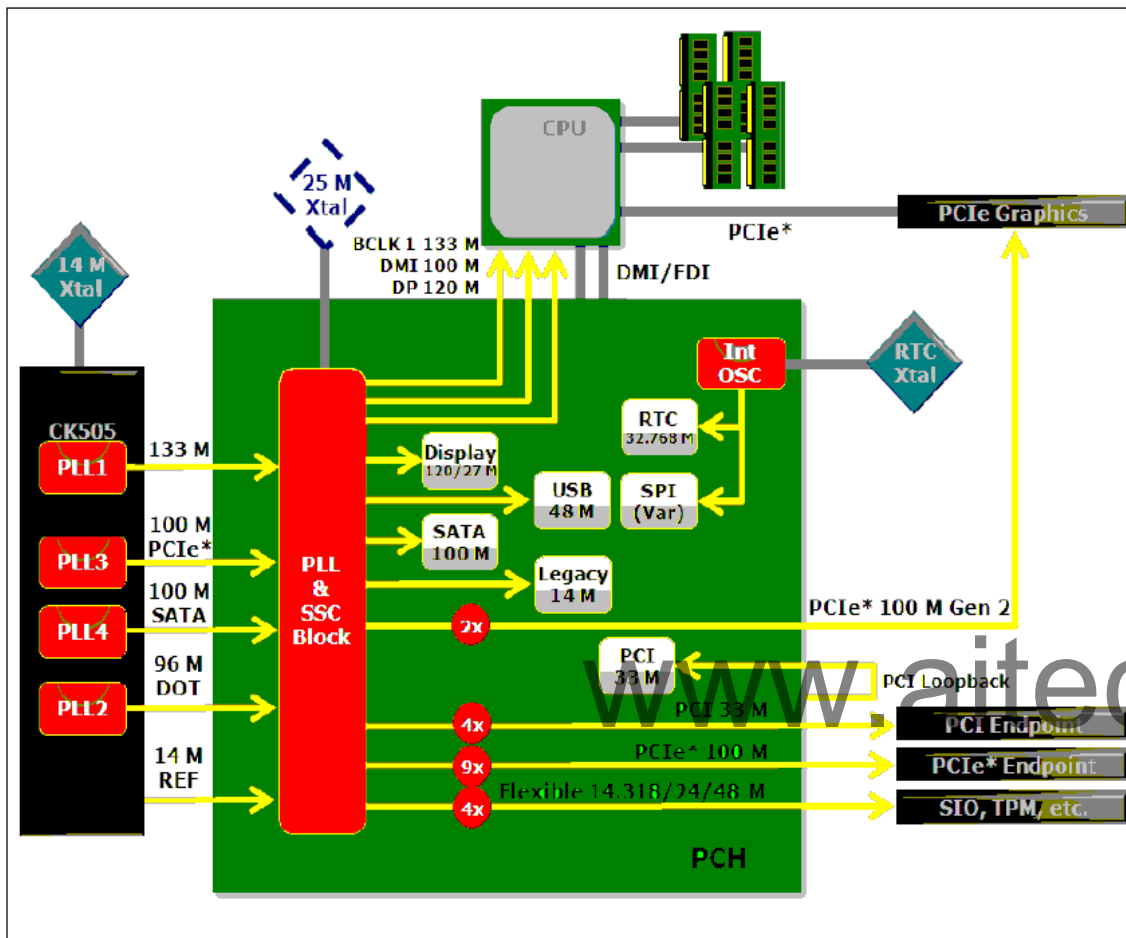


POWER SEQUENCE

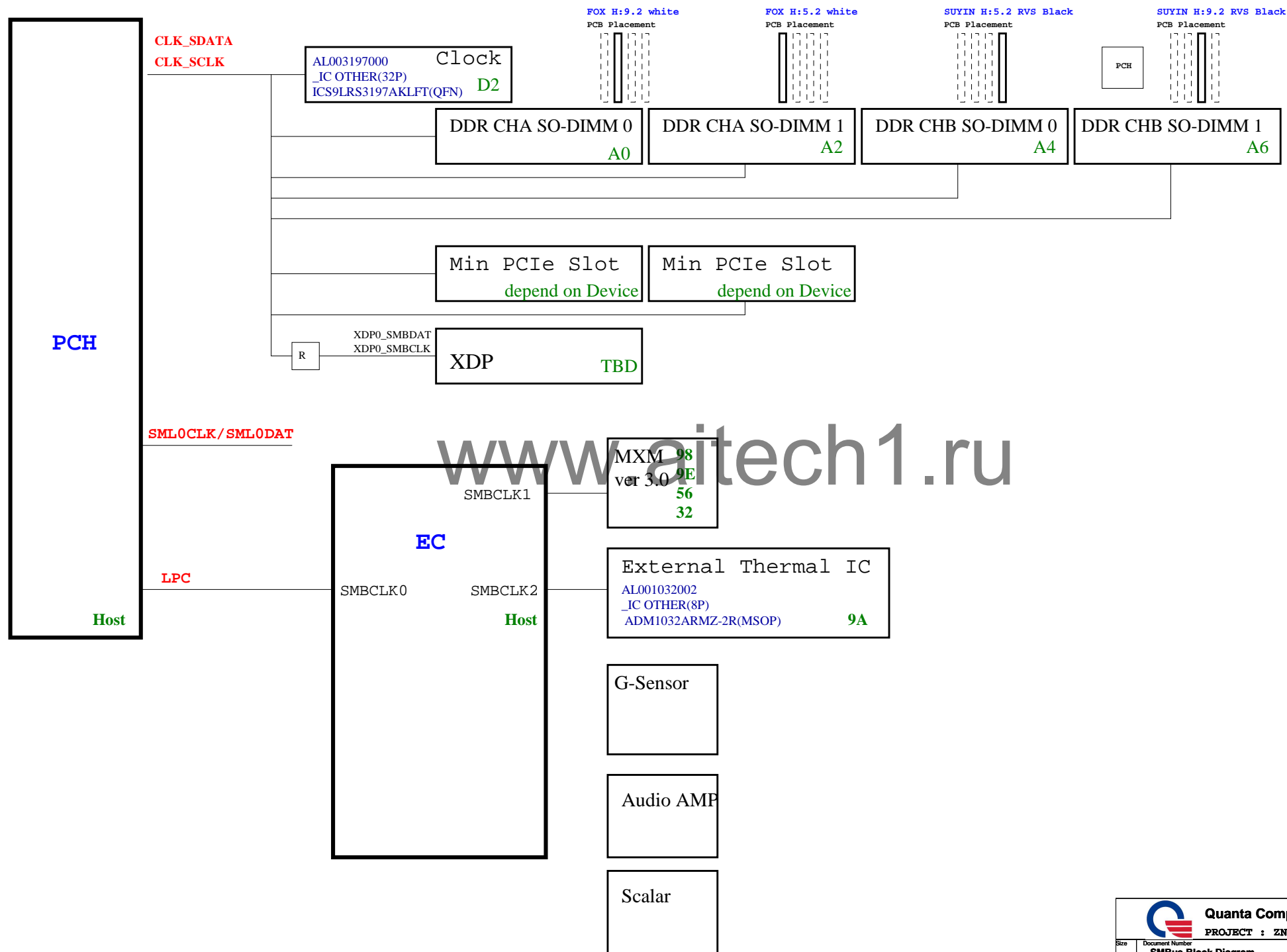
Voltage Rails

Power	Voltage	S0	S3	S4	S5	PCU	G3	Cri Signal
+VCCRTC	3V	ON	ON	ON	ON	ON	ON	
VIN	18.5V	ON	ON	ON	ON	ON	OFF	Adaptor In
+5VPCU	5V	ON	ON	ON	ON	ON	OFF	Adaptor In
+5VPCU	3.3V	ON	ON	ON	ON	ON	OFF	Adaptor In
+5V_S5	5V	ON	ON	ON	ON	OFF	OFF	S5_PWR_ON
+3V_S5	3.3V	ON	ON	ON	ON	OFF	OFF	S5_PWR_ON
+5V_S3	5V	ON	ON	OFF	OFF	OFF	OFF	S3_PWR_ON
+1.5V_S0S2	1.5V	ON	ON	OFF	OFF	OFF	OFF	S0S2_ON
S0S0R_VTSS0K	0.75V	ON	OFF	OFF	OFF	OFF	OFF	S0S0N
+12V	12V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
+5V	5V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
+3V	3.3V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
+1.5V	1.5V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
+1.05V	1.05V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
+1.8V	1.8V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
+1.1V_VTT	1.1V/1.05V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
V_AIO	777V	ON	OFF	OFF	OFF	OFF	OFF	GPIO_VIN_EN
+VCC_CORE	777V	ON	OFF	OFF	OFF	OFF	OFF	VIRON

[illegible]



ZN7 SMbus Block Diagram

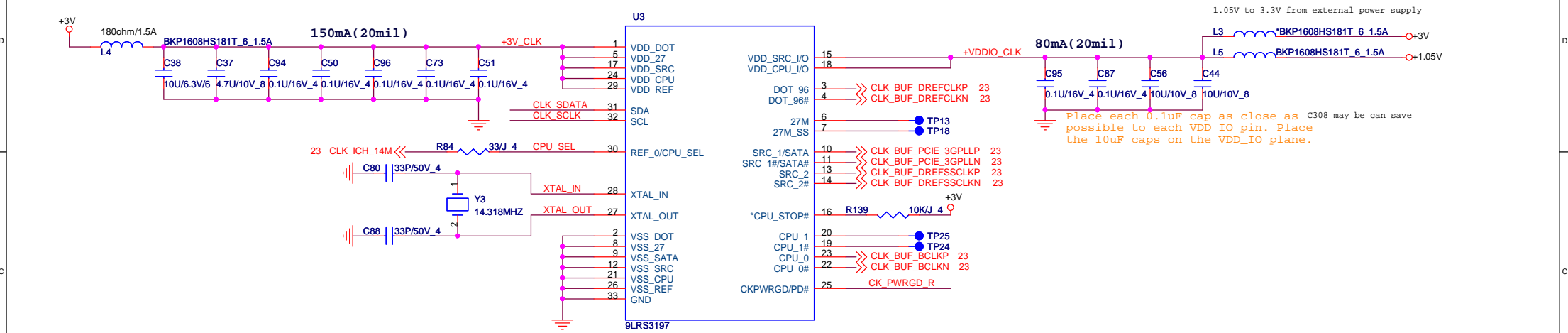


NAME	GPIO/PIN	I/O	DESCRIPTION	ACTIVE
		I		INITIAL : HIGH / ACTIVE : LOW
		B		
		I		
		I		
		O		
		O		
		I		
		O		
		O		
		O		
		O		
		I		
		O		
		O		
		O		
		O		
		O		
		I		
		I		
		I		
		I		
		I		
		I		
		I		
		I		
		O		
		O		
		O		
		I		
		I		

NAME	GPIO/PIN	I/O	DESCRIPTION	ACTIVE
		I		
		B		
		I		
		I		
		O		
		O		
		I		
		O		
		O		
		O		
		O		
		I		
		O		
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		O		
		I		
		I		

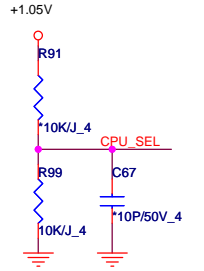
www.aitech1.ru

Clock Generator



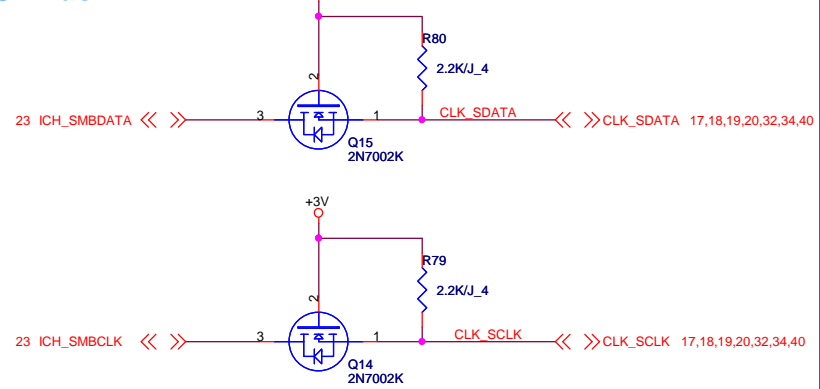
www.aitech1.ru

CPU_CLK select

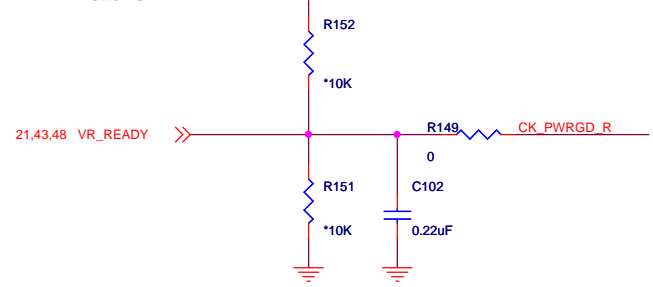



	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable



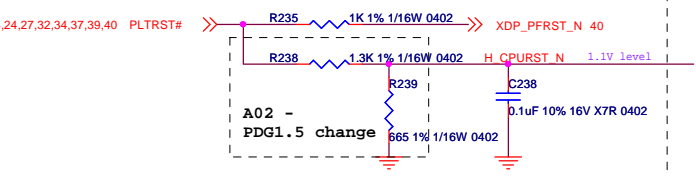
**Quanta Computer Inc.**
PROJECT : ZN9

Size	Document Number	Rev
	Clock Generator	F
Date:	Monday, March 29, 2010	Sheet 9 of 51

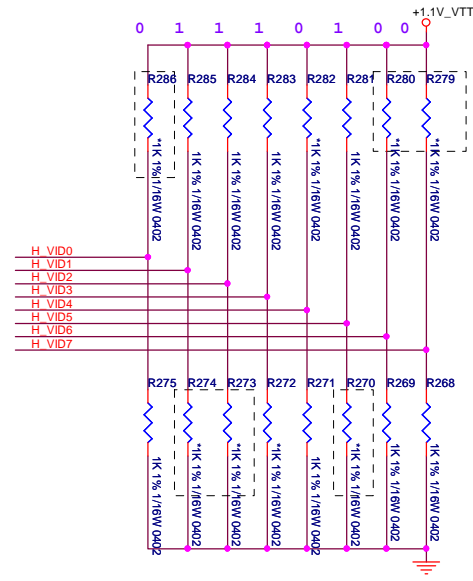
CFG	H	L	Notes
0			H:1x16, L:2x8
1	RSVD		
2	RSVD		
3	NORM	RSVD	LANE REVERSAL
4	DISABLE	ENABLE	DP PRESENCE
5	RSVD		
6	RSVD		

CFG 0-6 all internal PULL-UP

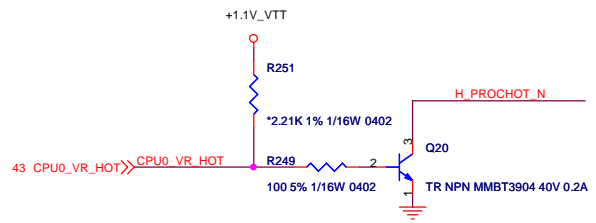
Need to be placed close to processor to minimize ESD risk

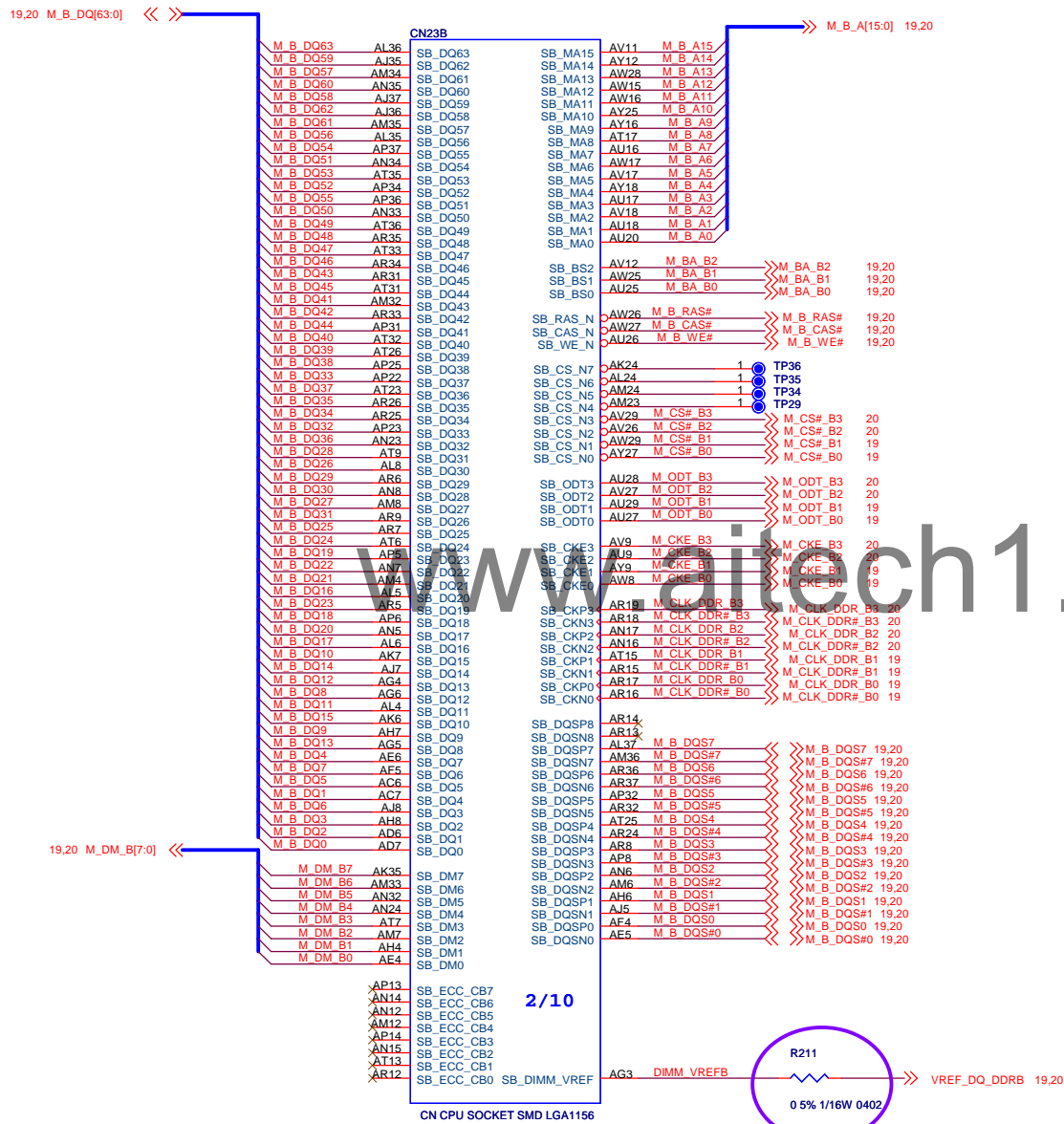


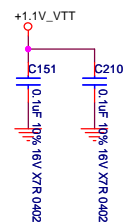
VID[7:0] : 00101110 =>1.325V@VCC_Max
2009B FMB processors supported



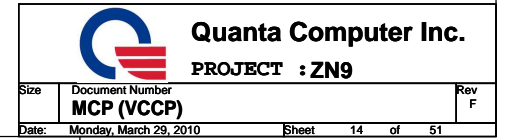
CAD NOTE:
PLACE TDO TERMINATION NEAR XDP CONNECTOR
PLACE TCK/TDI/TMS END TERMINATION NEAR CPU

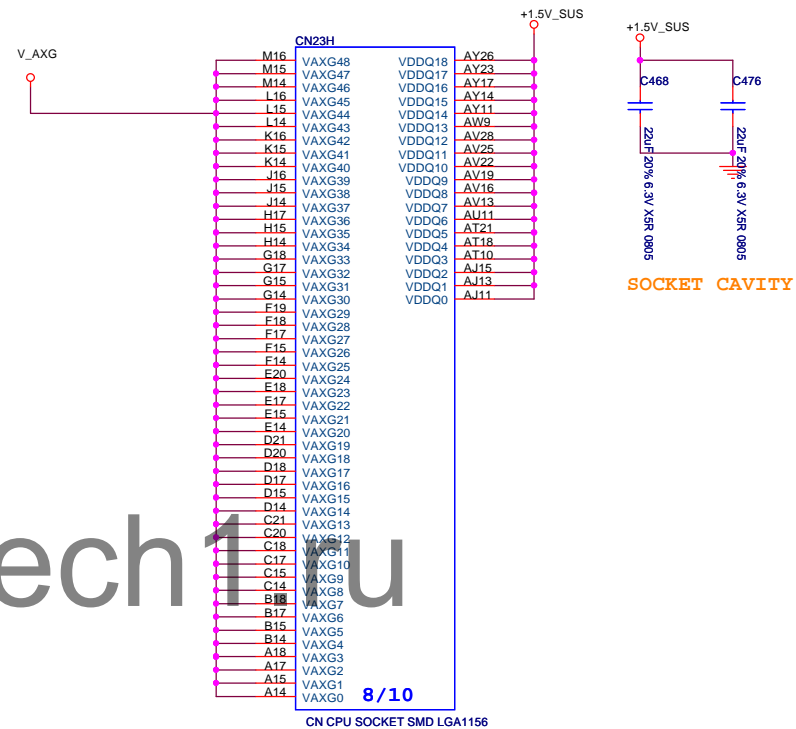
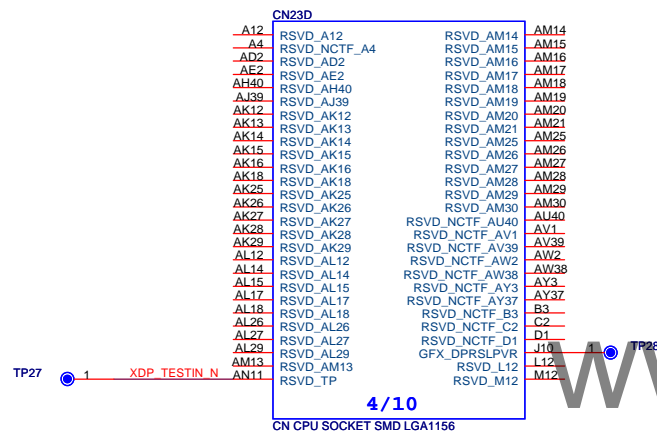


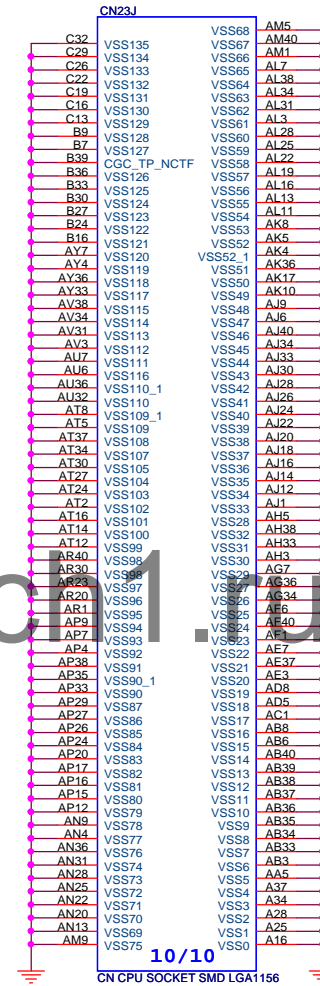
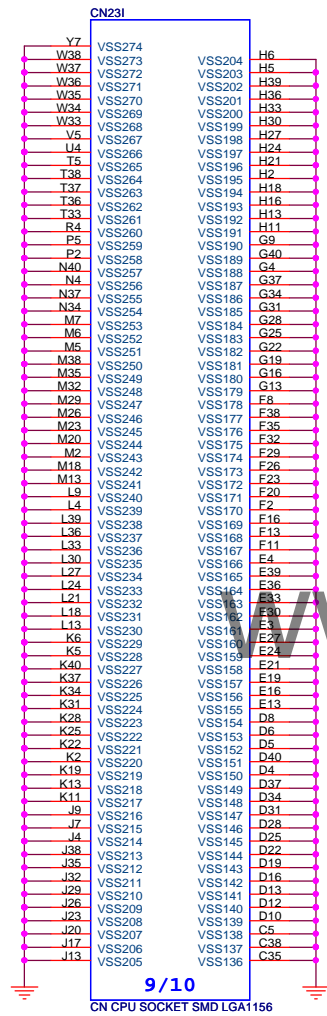




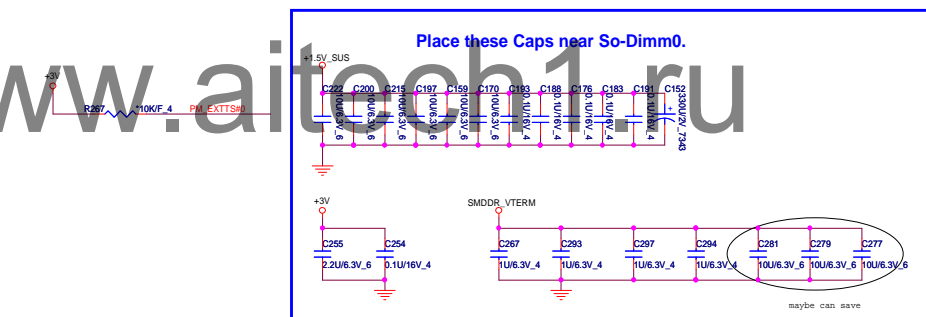
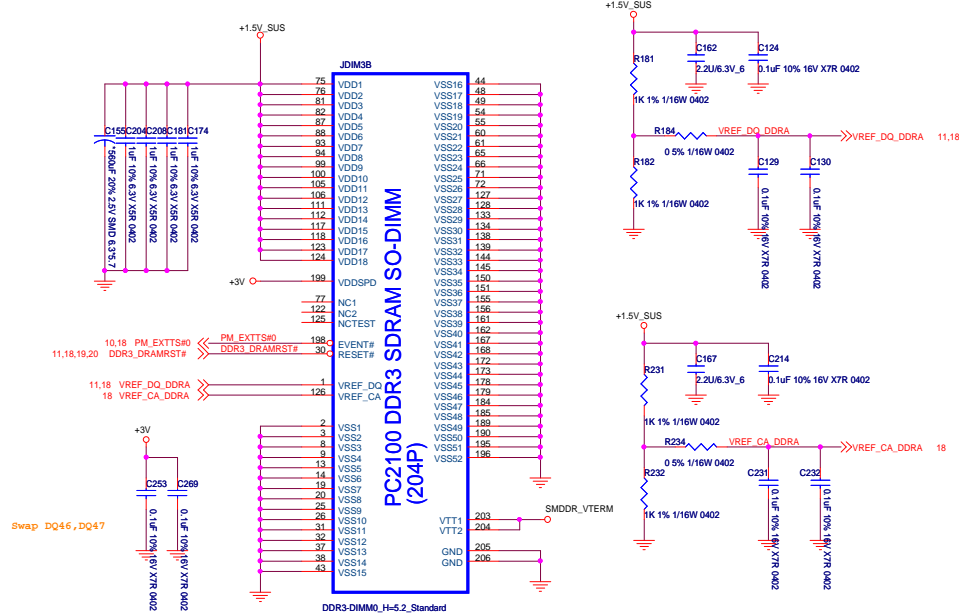
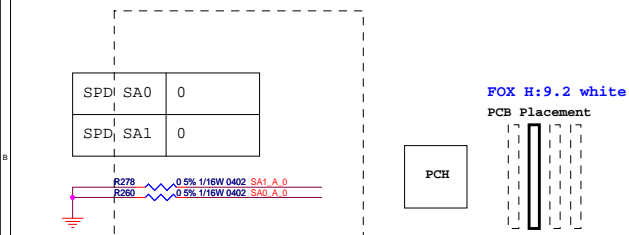
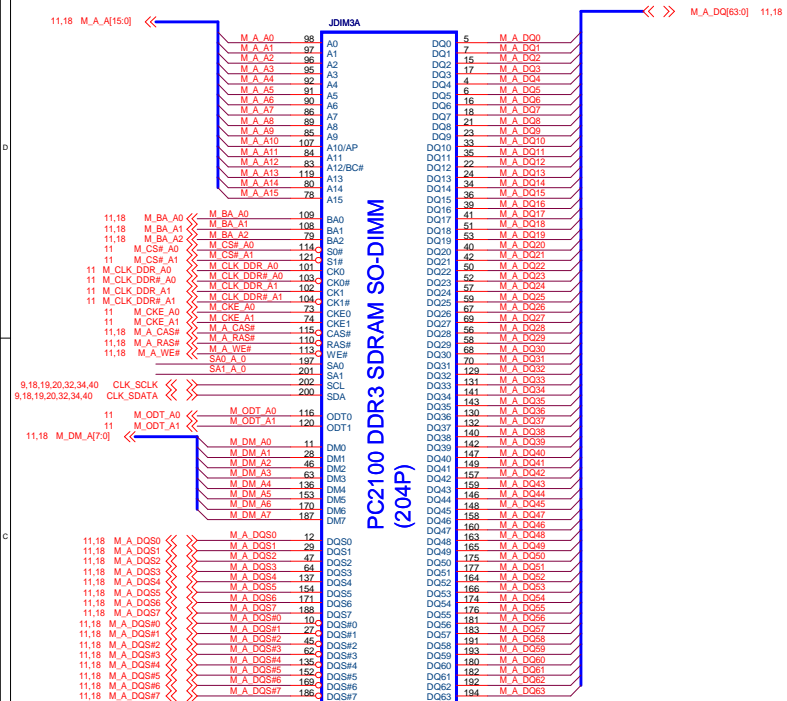
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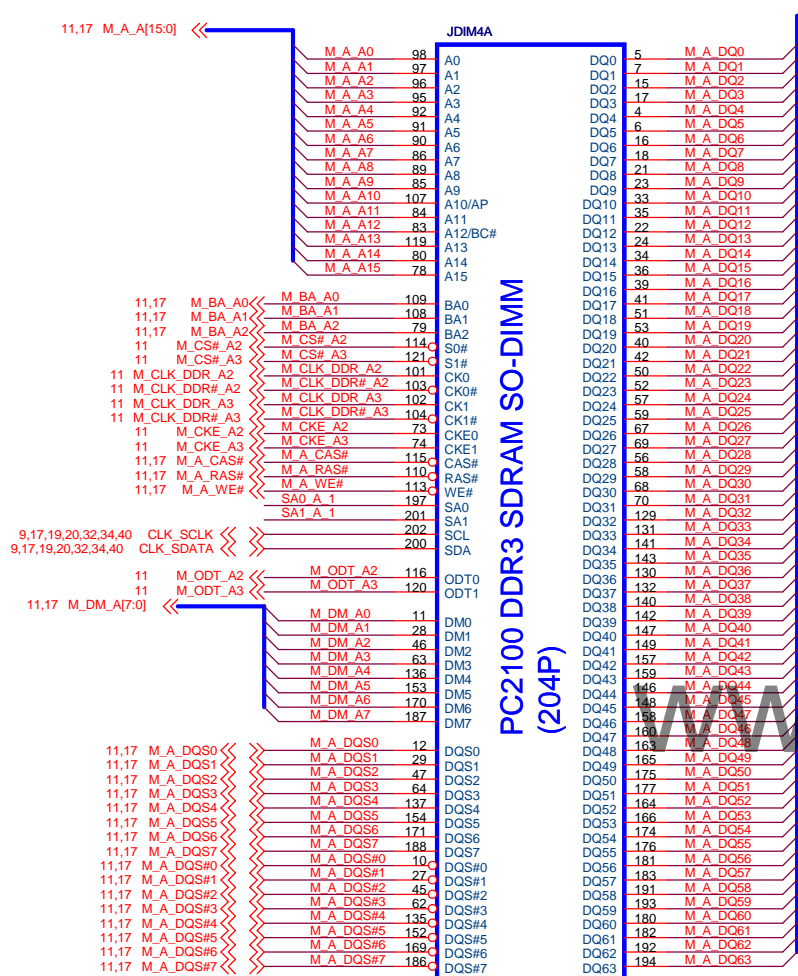




CHANNEL A DIMM 0



CHANNEL A DIMM 1



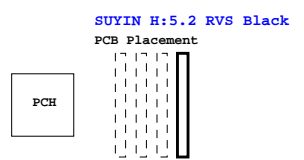
SPD SA0 0

SPD SA1 1

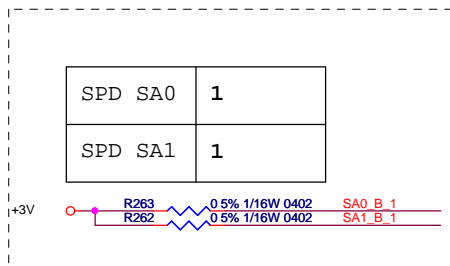
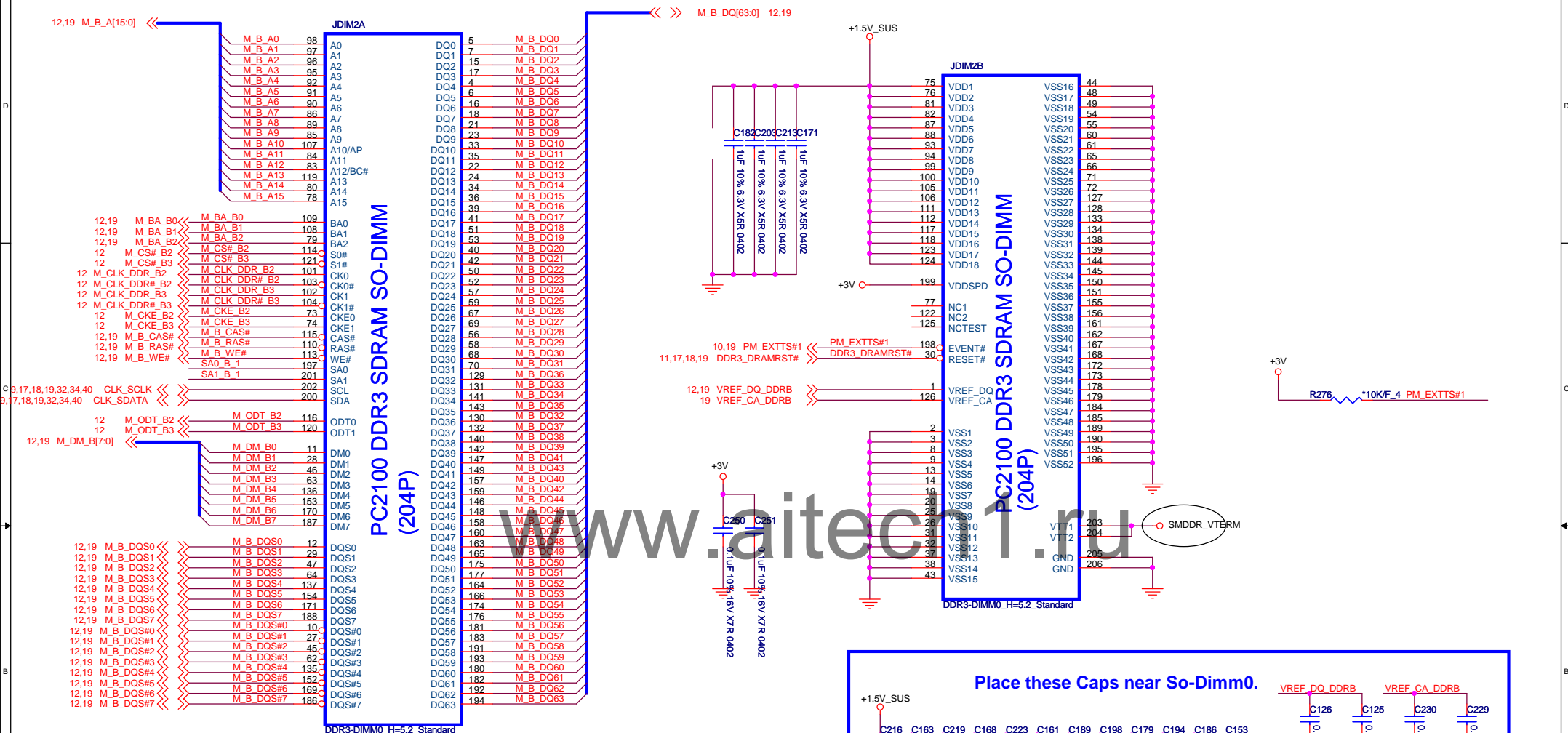
3V

R277 0 5% 1/16W 0402 SA0_B_0

R259 0 5% 1/16W 0402 SA1_B_0

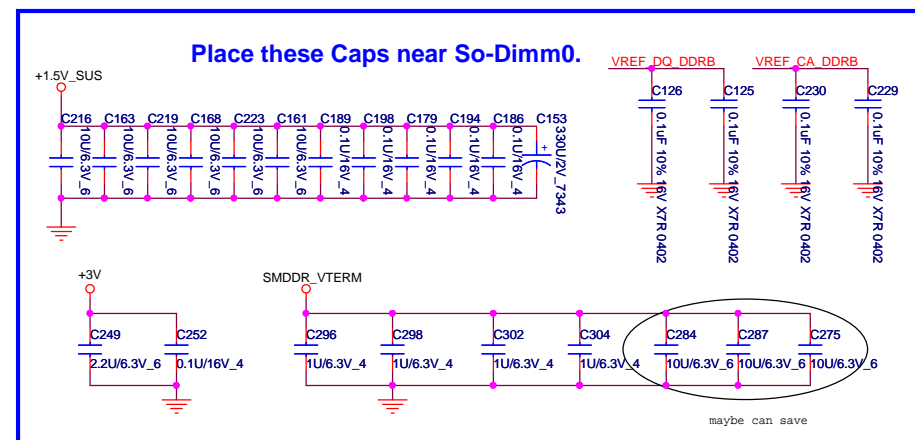


CHANNEL B DIMM 3



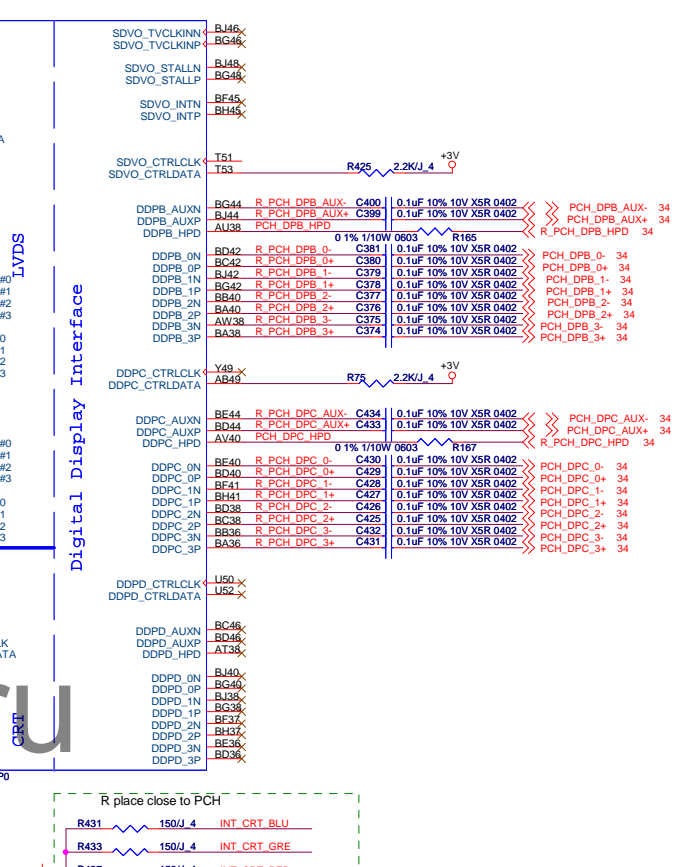
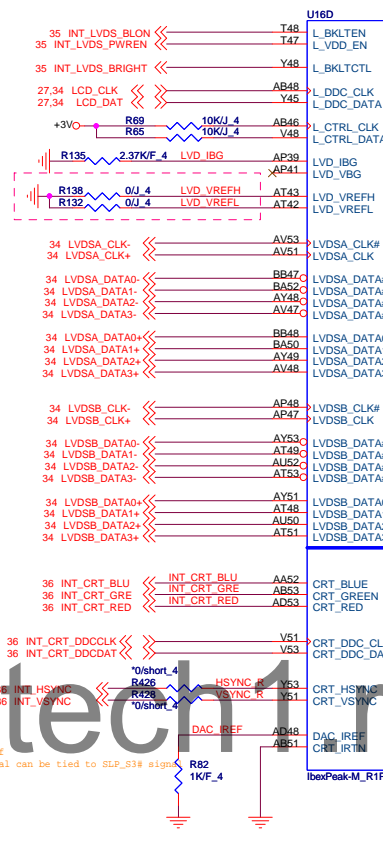
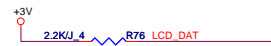
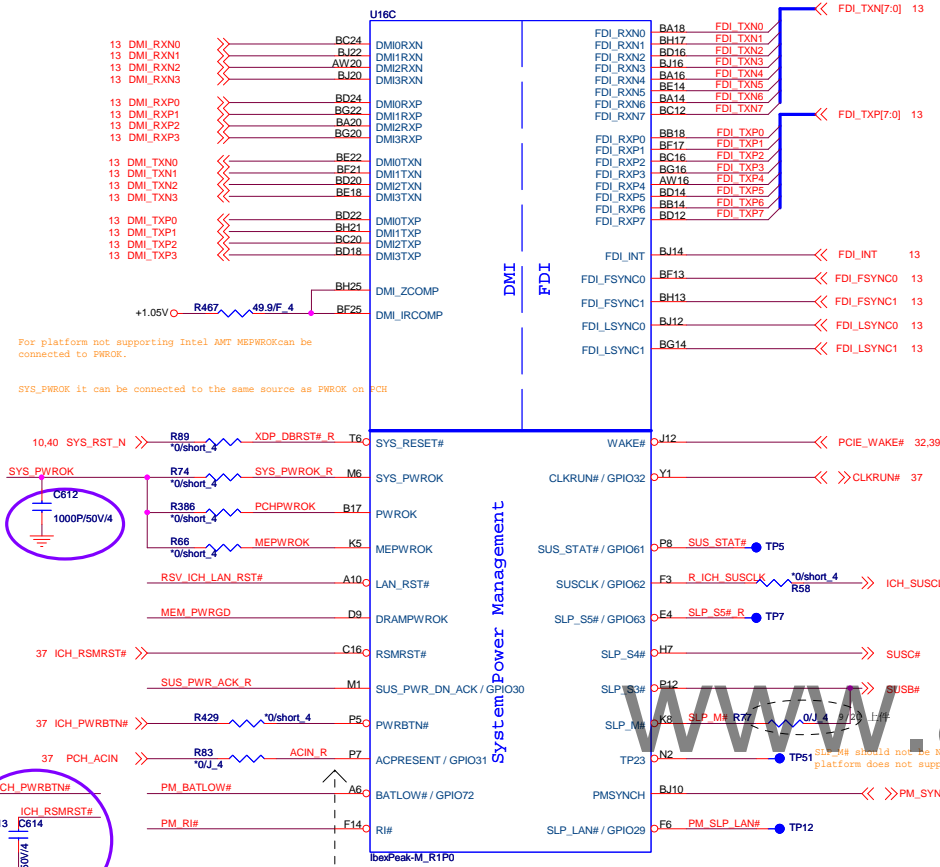
SUYIN H:9.2 RVS Black

PCB Placement

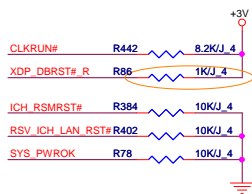


IBEX PEAK-M (DMI,FDI,GPIO)

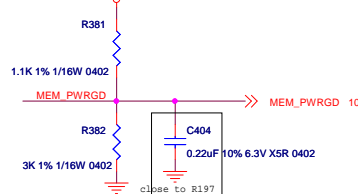
IBEX PEAK-M (LVDS,DDI)



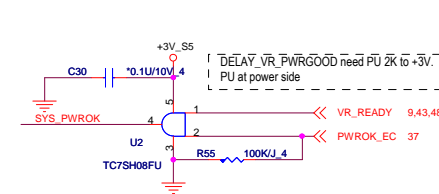
PCH Pull-high/low

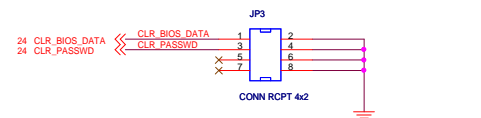


DRAMWROK



System PWR_OK



[illegible]

28 PCH_AZ_CODEC_SYNC R388 33.4k ACZ_SYNC
 R389 33.4

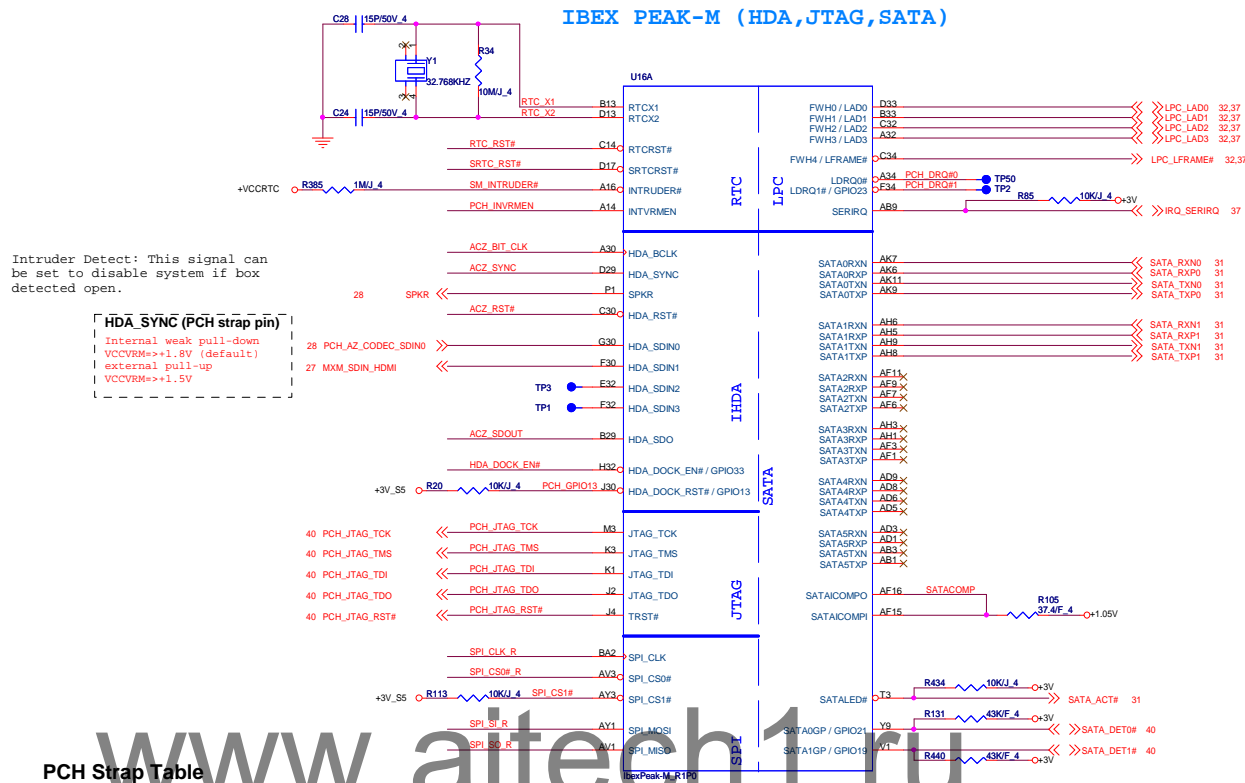
29 PCH_AZ_CODEC_RST# R394 33.4k ACZ_RST#
 R395 33.4





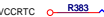















30 PCH_AZ_CODEC_SDOUT R390 33.4k ACZ_SDOUT
 R391 33.4

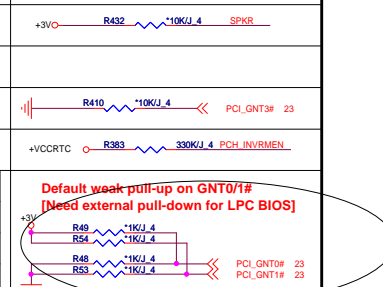
28 PCH_AZ_CODEC_BITCLK R392 33.4k ACZ_BIT_CLK
 29 PCH_AZ_CODEC_BITCLK_ R393 33.4

C397 C398
 27pF_4 27pF_4

Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

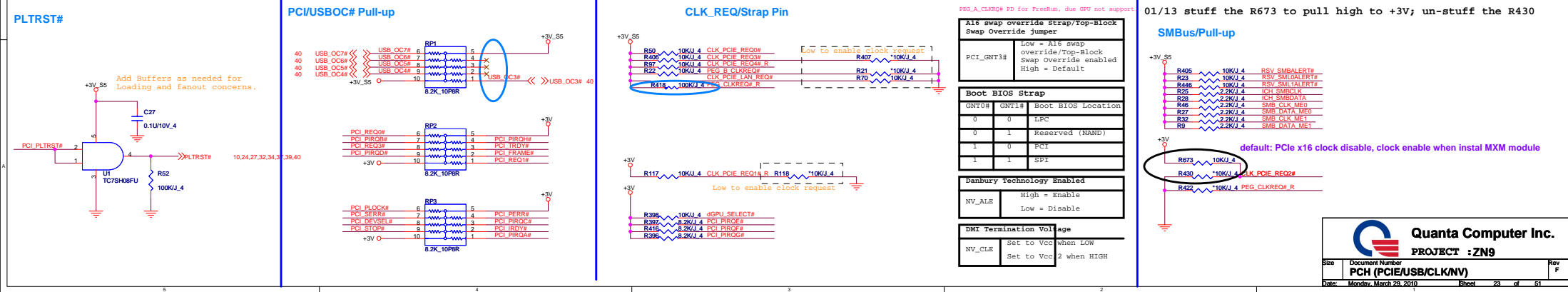
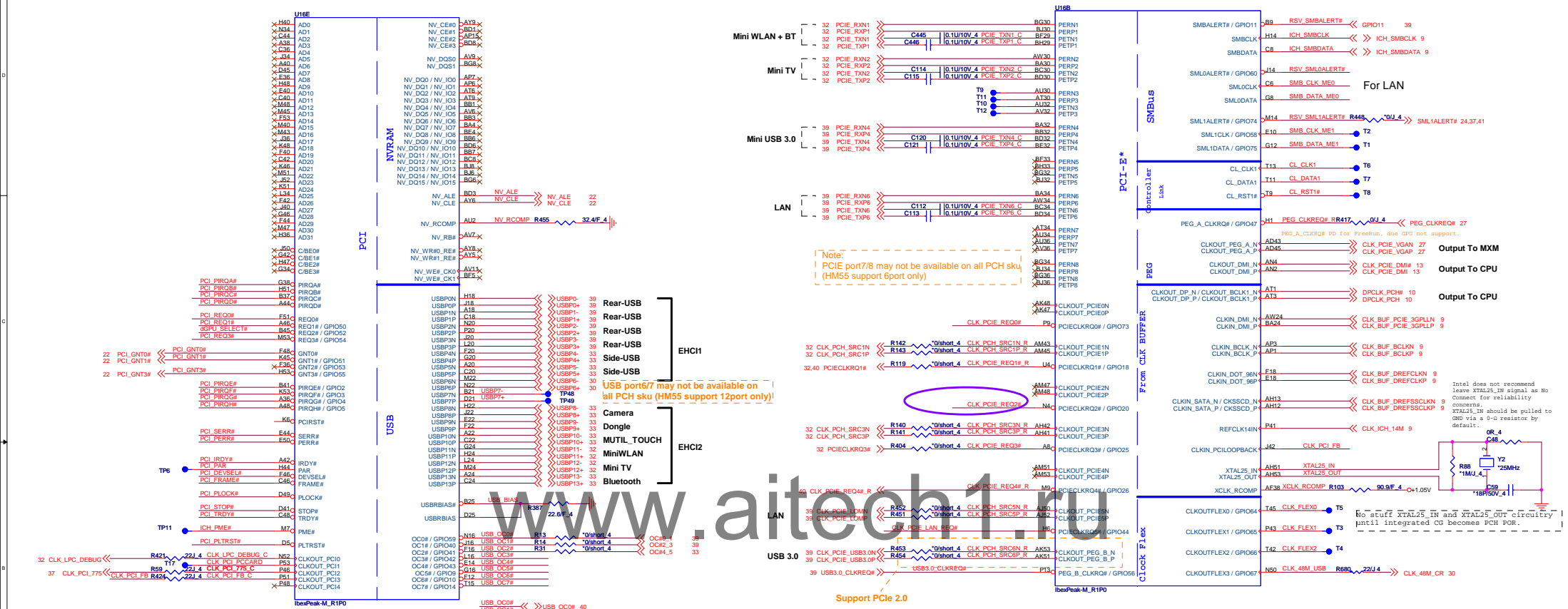


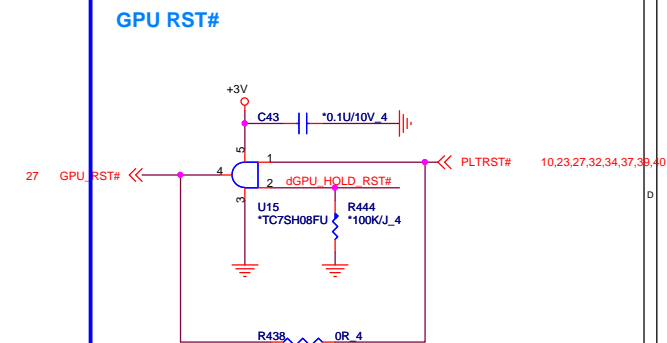
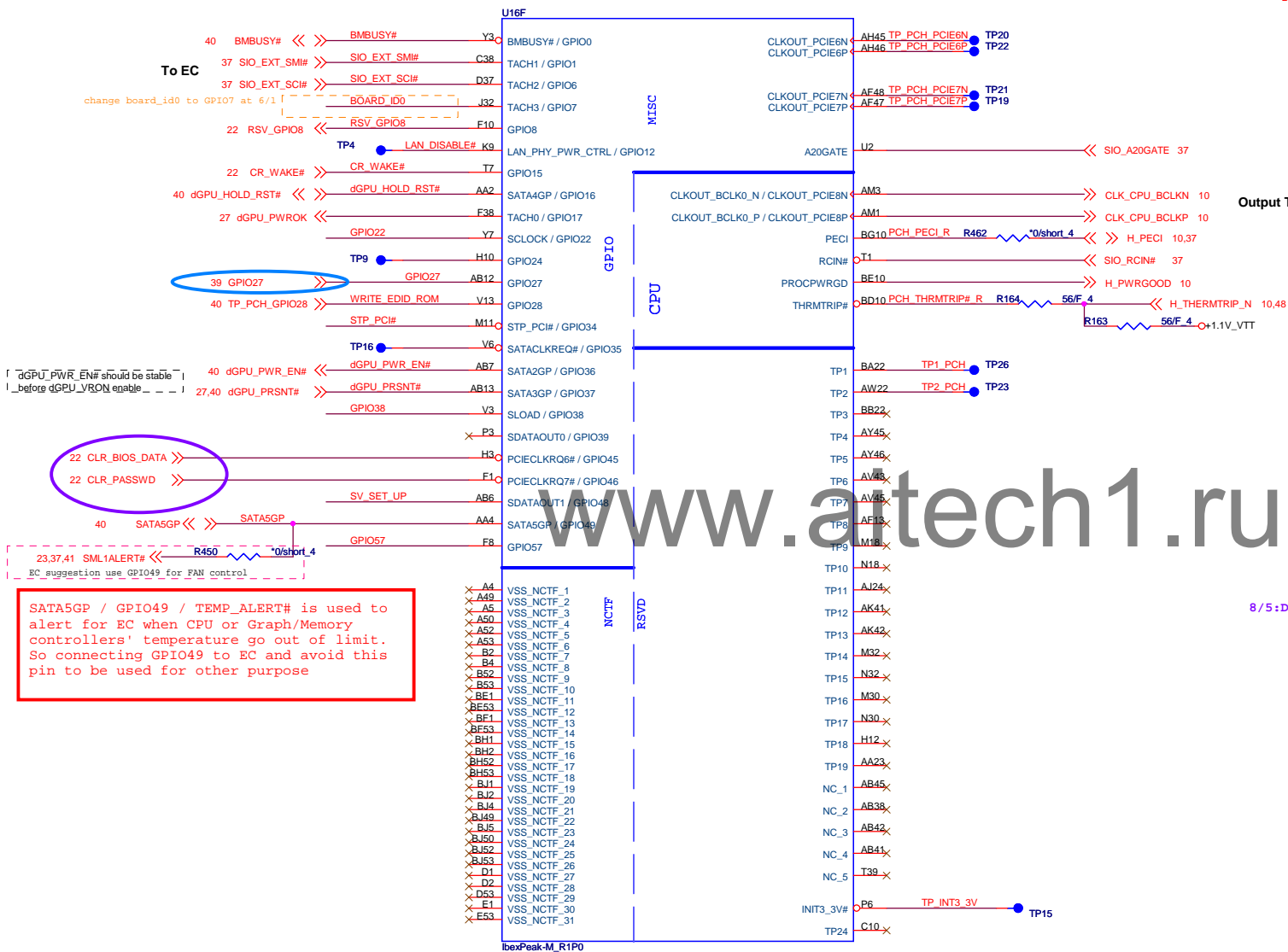
Pin Name	Strap description	Sampled	Configuration	ZN7 note												
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V○  *10KJ_4  SPKR												
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down													
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	 *10KJ_4  PCI_GNT3# 23												
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+VCCRTC ○  330KJ_4  PCH_INVRMEN												
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr> </thead> <tbody> <tr> <td>1</td><td>1</td><td>SPI</td></tr> <tr> <td>1</td><td>0</td><td>PCI</td></tr> <tr> <td>0</td><td>0</td><td>LPC</td></tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI	1	0	PCI	0	0	LPC	<p>Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]</p> 
GNT1#	GNT0#	Boot Location														
1	1	SPI														
1	0	PCI														
0	0	LPC														
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK														
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN												
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V○  *1KJ_4  NV_ALE 23												
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V○  *1KJ_4  NV_CLE 23												
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	 *1KJ_4  HDA_DOCK_EN#												
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V○  *1KJ_4  SPI_SI_R												
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)													
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_SS ○  10KJ_4  RSV_GPIO8 2												
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)													
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use default (0 = 1.8V supply)												
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	+3V_SS ○  1KJ_4  CR_WAKE# 24												



IBEX PEAK-M (PCI,USB,NVRAM)

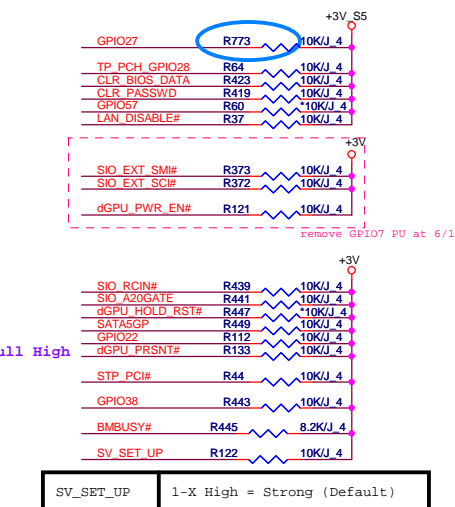
IBEX PEAK-M (PCI-E,SMBUS,CLK)



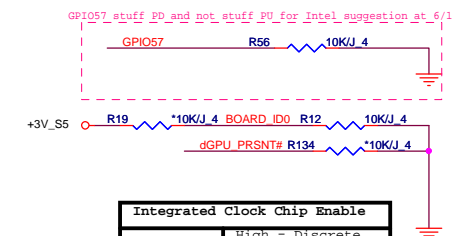


Output To CPU

GPIO Pull-up/Pull-down

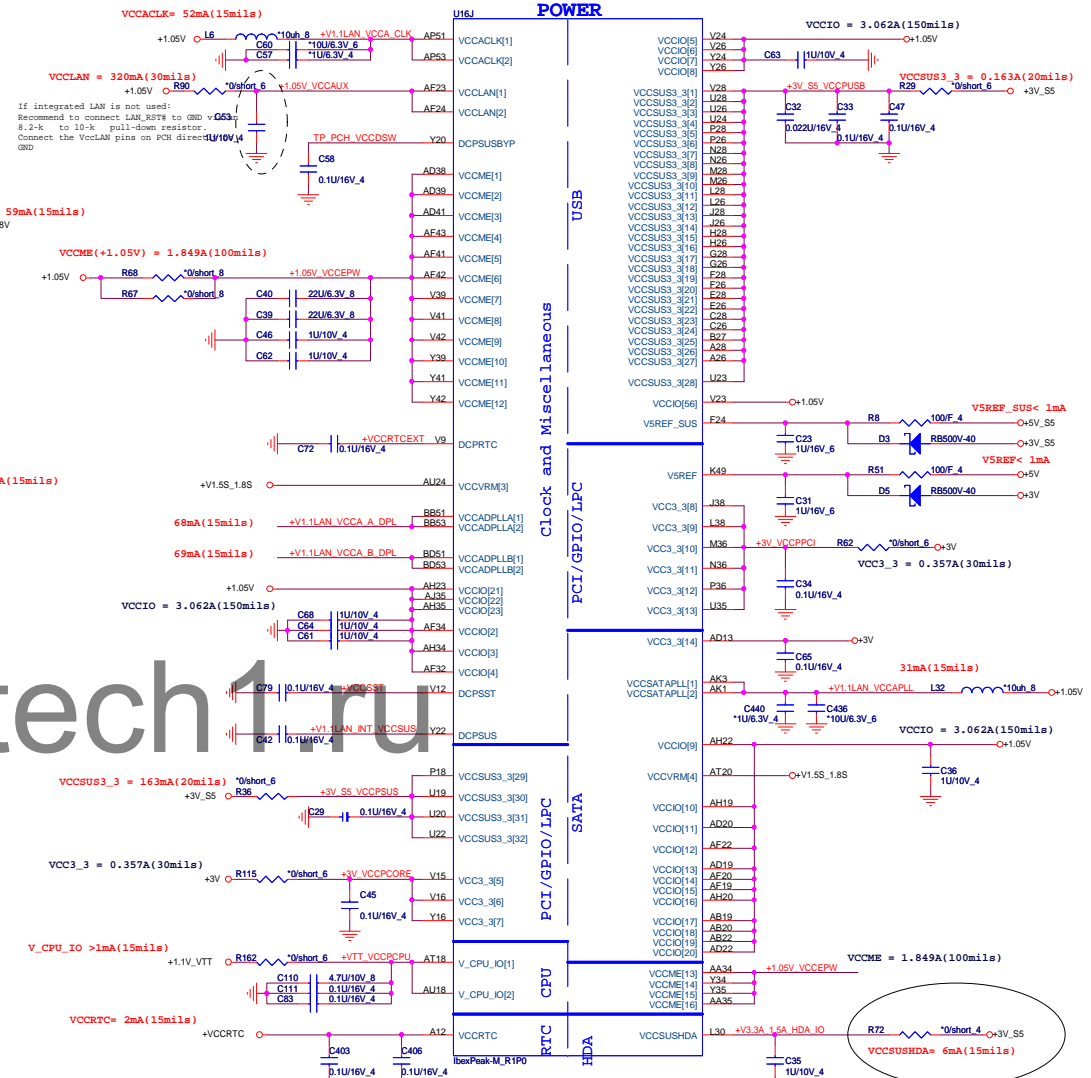
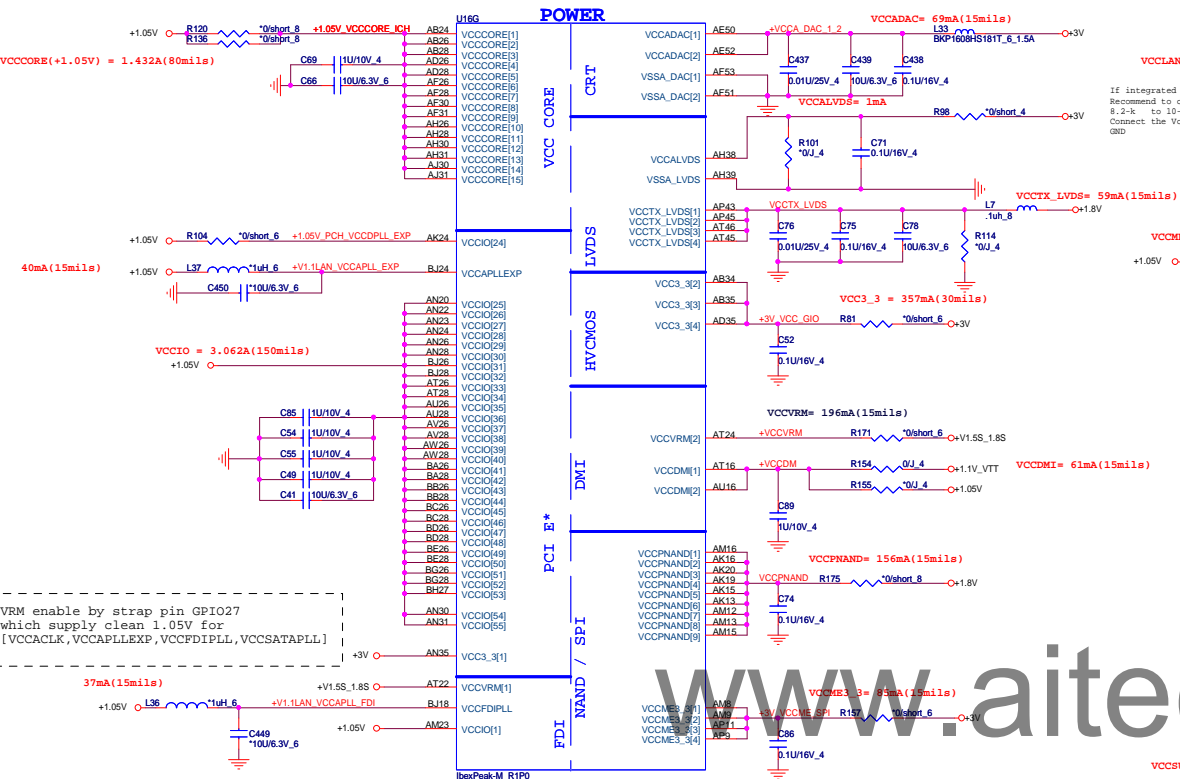


8/5:Default Pull High



Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = SW
RSV_GPIO8	High = Disable Low = Enable

IBEX PEAK-M (POWER)



IBEX PEAK-M (GND)

U16H		
AB16	VSS[0]	
AA19	VSS[1]	VSS[80]
AA20	VSS[2]	VSS[81]
AA22	VSS[3]	VSS[82]
AM19	VSS[4]	VSS[83]
AA24	VSS[5]	VSS[84]
AA26	VSS[6]	VSS[85]
AA28	VSS[7]	VSS[86]
AA30	VSS[8]	VSS[87]
AA31	VSS[9]	VSS[88]
AA32	VSS[10]	VSS[89]
AB11	VSS[11]	VSS[90]
AB15	VSS[12]	VSS[91]
AB23	VSS[13]	VSS[92]
AB30	VSS[14]	VSS[93]
AB31	VSS[15]	VSS[94]
AB32	VSS[16]	VSS[95]
AB39	VSS[17]	VSS[96]
AB43	VSS[18]	VSS[97]
AB47	VSS[19]	VSS[98]
AB5	VSS[20]	VSS[99]
AC2	VSS[21]	VSS[100]
AC52	VSS[22]	VSS[101]
AD11	VSS[23]	VSS[102]
AD12	VSS[24]	VSS[103]
AD16	VSS[25]	VSS[104]
AD23	VSS[26]	VSS[105]
AD30	VSS[27]	VSS[106]
AD31	VSS[28]	VSS[107]
AD32	VSS[29]	VSS[108]
AD34	VSS[30]	VSS[109]
AD39	VSS[31]	VSS[110]
AD42	VSS[32]	VSS[111]
AD44	VSS[33]	VSS[112]
AD49	VSS[34]	VSS[113]
AD7	VSS[35]	VSS[114]
AE2	VSS[36]	VSS[115]
AE4	VSS[37]	VSS[116]
AE12	VSS[38]	VSS[117]
Y13	VSS[39]	VSS[118]
AH49	VSS[40]	VSS[119]
AF36	VSS[41]	VSS[120]
AN34	VSS[42]	VSS[121]
AF45	VSS[43]	VSS[122]
AF46	VSS[44]	VSS[123]
AF49	VSS[45]	VSS[124]
AF5	VSS[46]	VSS[125]
AG2	VSS[47]	VSS[126]
AG52	VSS[48]	VSS[127]
AH11	VSS[49]	VSS[128]
AH15	VSS[50]	VSS[129]
AH16	VSS[51]	VSS[130]
AH24	VSS[52]	VSS[131]
AH32	VSS[53]	VSS[132]
AV18	VSS[54]	VSS[133]
AH43	VSS[55]	VSS[134]
AH47	VSS[56]	VSS[135]
AH7	VSS[57]	VSS[136]
AJ19	VSS[58]	VSS[137]
AJ2	VSS[59]	VSS[138]
AJ20	VSS[60]	VSS[139]
AJ22	VSS[61]	VSS[140]
AJ23	VSS[62]	VSS[141]
AJ26	VSS[63]	VSS[142]
AJ28	VSS[64]	VSS[143]
AJ32	VSS[65]	VSS[144]
AJ34	VSS[66]	VSS[145]
AJ4	VSS[67]	VSS[146]
AK12	VSS[68]	VSS[147]
AM41	VSS[69]	VSS[148]
AN19	VSS[70]	VSS[149]
AK26	VSS[71]	VSS[150]
AK22	VSS[72]	VSS[151]
AK28	VSS[73]	VSS[152]
AK29	VSS[74]	VSS[153]
AK30	VSS[75]	VSS[154]
AK31	VSS[76]	VSS[155]
AK32	VSS[77]	VSS[156]
AK33	VSS[78]	VSS[157]
AK34	VSS[79]	VSS[158]

IbexPeak-M_R1P0

U16I		
AY7	VSS[159]	VSS[259]
B11	VSS[160]	VSS[260]
B15	VSS[161]	VSS[261]
B19	VSS[162]	VSS[262]
B23	VSS[163]	VSS[263]
B31	VSS[164]	VSS[264]
B35	VSS[165]	VSS[265]
B39	VSS[166]	VSS[266]
B43	VSS[167]	VSS[267]
B47	VSS[168]	VSS[268]
B7	VSS[169]	VSS[269]
BG12	VSS[170]	VSS[270]
BB12	VSS[171]	VSS[271]
BB16	VSS[172]	VSS[272]
BB20	VSS[173]	VSS[273]
BB24	VSS[174]	VSS[274]
BB30	VSS[175]	VSS[275]
BB34	VSS[176]	VSS[276]
BB38	VSS[177]	VSS[277]
BB42	VSS[178]	VSS[278]
BB49	VSS[179]	VSS[279]
BB5	VSS[180]	VSS[280]
BC10	VSS[181]	VSS[281]
BC14	VSS[182]	VSS[282]
BC18	VSS[183]	VSS[283]
BC2	VSS[184]	VSS[284]
BC22	VSS[185]	VSS[285]
BC32	VSS[186]	VSS[286]
BC36	VSS[187]	VSS[287]
BC40	VSS[188]	VSS[288]
BC44	VSS[189]	VSS[289]
BC52	VSS[190]	VSS[290]
BH9	VSS[191]	VSS[291]
BD48	VSS[192]	VSS[292]
BD49	VSS[193]	VSS[293]
BD5	VSS[194]	VSS[294]
BE12	VSS[195]	VSS[295]
BE16	VSS[196]	VSS[296]
BE20	VSS[197]	VSS[297]
BE24	VSS[198]	VSS[298]
BE30	VSS[199]	VSS[299]
BE34	VSS[200]	VSS[300]
BE38	VSS[201]	VSS[301]
BE42	VSS[202]	VSS[302]
BE46	VSS[203]	VSS[303]
BE48	VSS[204]	VSS[304]
BE50	VSS[205]	VSS[305]
BE6	VSS[206]	VSS[306]
BE8	VSS[207]	VSS[307]
BE9	VSS[208]	VSS[308]
BE49	VSS[209]	VSS[309]
BE51	VSS[210]	VSS[310]
BG14	VSS[211]	VSS[311]
BG24	VSS[212]	VSS[312]
BG4	VSS[213]	VSS[313]
BG50	VSS[214]	VSS[314]
BH11	VSS[215]	VSS[315]
BH15	VSS[216]	VSS[316]
BH19	VSS[217]	VSS[317]
BH23	VSS[218]	VSS[318]
BH31	VSS[219]	VSS[319]
BH35	VSS[220]	VSS[320]
BH39	VSS[221]	VSS[321]
BH43	VSS[222]	VSS[322]
BH47	VSS[223]	VSS[323]
C12	VSS[224]	VSS[324]
C32	VSS[225]	VSS[325]
C50	VSS[226]	VSS[326]
D51	VSS[227]	VSS[327]
E12	VSS[228]	VSS[328]
E16	VSS[229]	VSS[329]
E20	VSS[230]	VSS[330]
E24	VSS[231]	VSS[331]
E30	VSS[232]	VSS[332]
E34	VSS[233]	VSS[333]
E38	VSS[234]	VSS[334]
E42	VSS[235]	VSS[335]
E46	VSS[236]	VSS[336]
E48	VSS[237]	VSS[337]
E6	VSS[238]	VSS[338]
E8	VSS[239]	VSS[339]
F49	VSS[240]	VSS[340]
F5	VSS[241]	VSS[341]
G10	VSS[242]	VSS[342]
G14	VSS[243]	VSS[343]
G18	VSS[244]	VSS[344]
G2	VSS[245]	VSS[345]
G22	VSS[246]	VSS[346]
G32	VSS[247]	VSS[347]
G36	VSS[248]	VSS[348]
G40	VSS[249]	VSS[349]
G44	VSS[250]	VSS[350]
G52	VSS[251]	VSS[351]
AF39	VSS[252]	VSS[352]
H16	VSS[253]	VSS[353]
H20	VSS[254]	VSS[354]
H30	VSS[255]	VSS[355]
H34	VSS[256]	VSS[356]
H38	VSS[257]	VSS[357]
H42	VSS[258]	VSS[358]

IbexPeak-M_R1P0

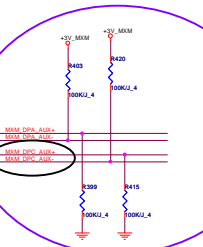
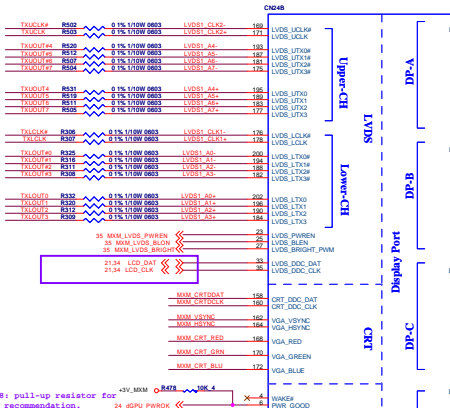
H49		
H5	J24	
K11	K43	
K47	K7	
L14	L18	
L2	L22	
L32	L36	
L40	L52	
M12	M16	
M20	M34	
M38	M42	
M46	M49	
M5	M8	
N24	P11	
AD15	P22	
P30	P32	
P34	P42	
P45	P47	
R2	R52	
T12	T41	
T46	T49	
T5	T8	
U30	U31	
U32	U34	
P38	P11	
P16	P19	
V12	V20	
V22	V32	
V30	V31	
V32	V34	
V38	V43	
V45	V46	
V49	V7	
V5	V8	
V7	V8	
W52	Y11	
Y12	Y15	
Y19	Y23	
Y23	Y28	
Y30	Y31	
Y32	Y38	
Y46	Y49	
P49	Y5	
Y6	Y8	
P24	T43	
AD51	AT8	
AT8	AD47	
AT12	AT13	
AM6	AM5	
AK45	AK39	
AV14		



Quanta Computer Inc.
PROJECT :ZN9

Size	Document Number	Rev
	PCH (GND)	F
Date:	Monday, March 29, 2010	Sheet 26 of 51

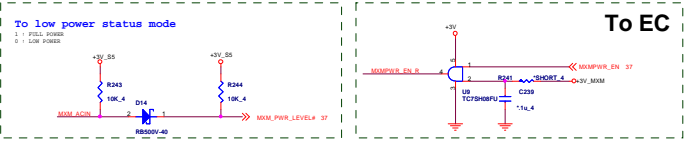
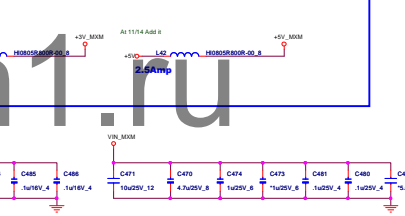
Check Footprint and P/N



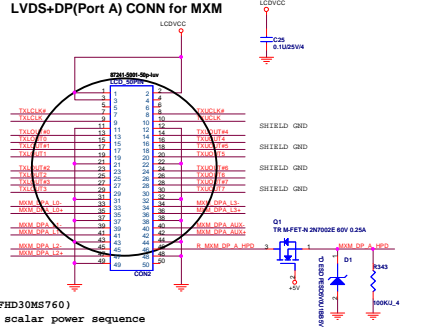
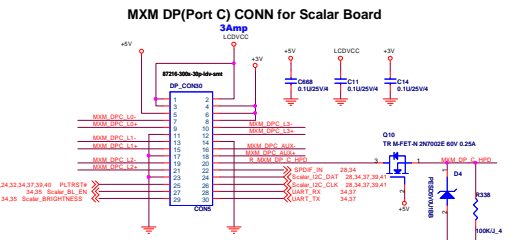
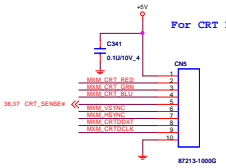
MXM VIN Power switch



MXM 3V/5V Power switch

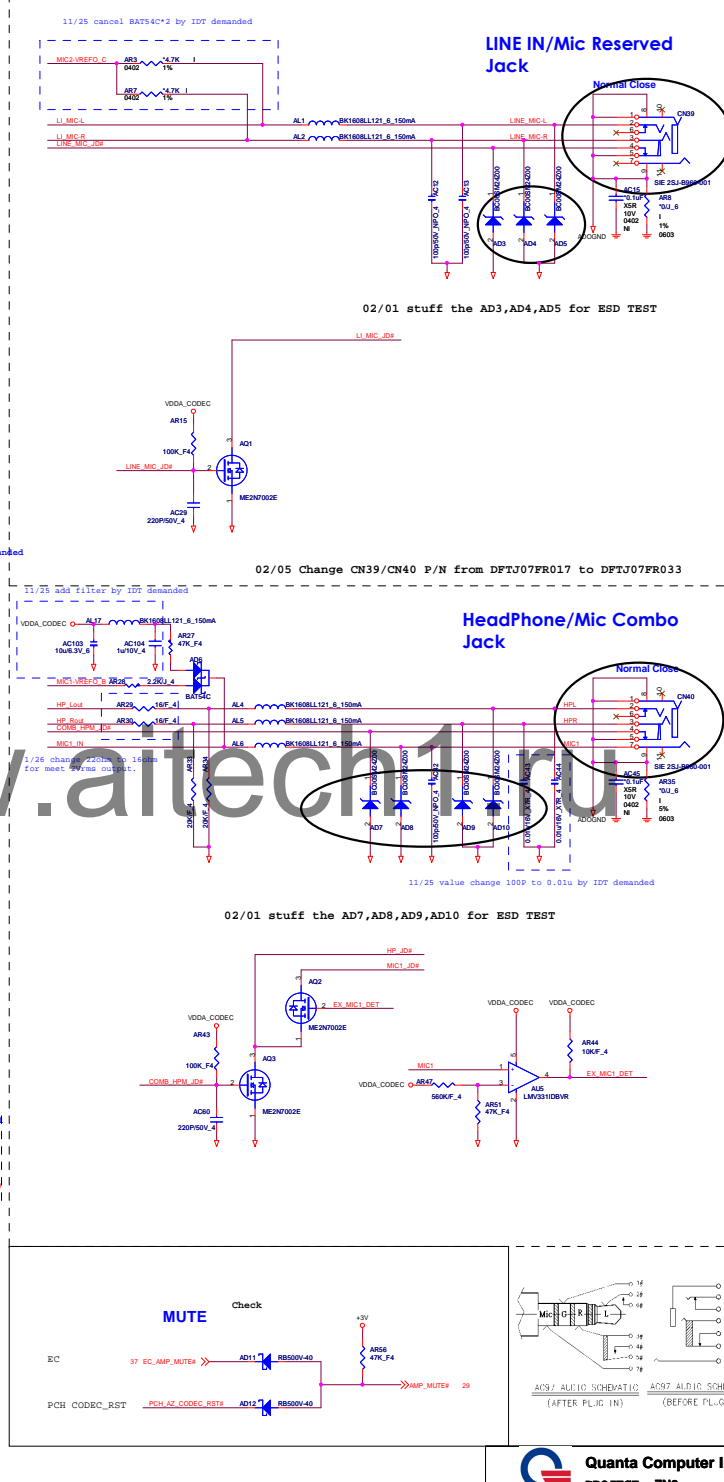
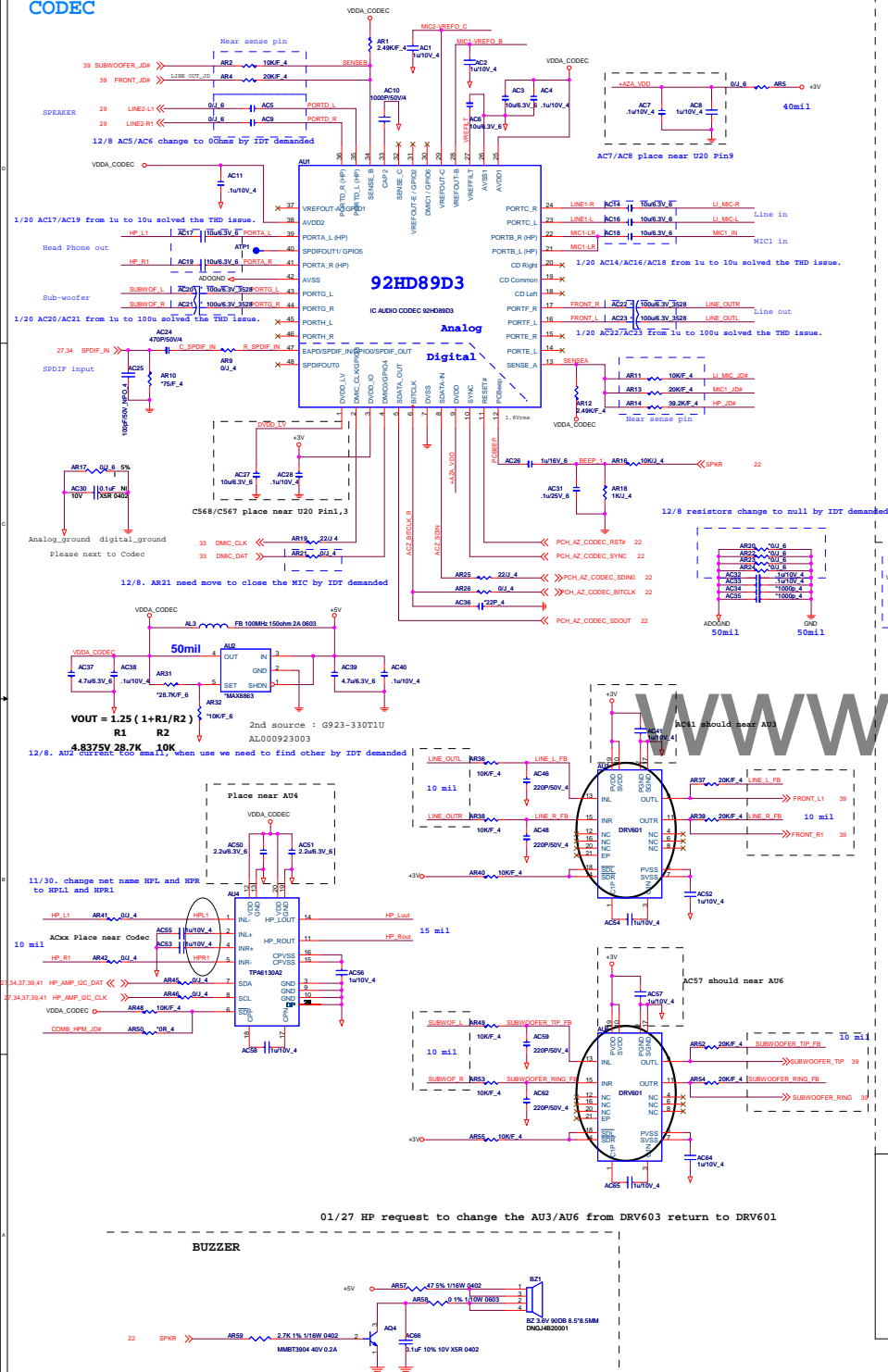


For CRT Debug



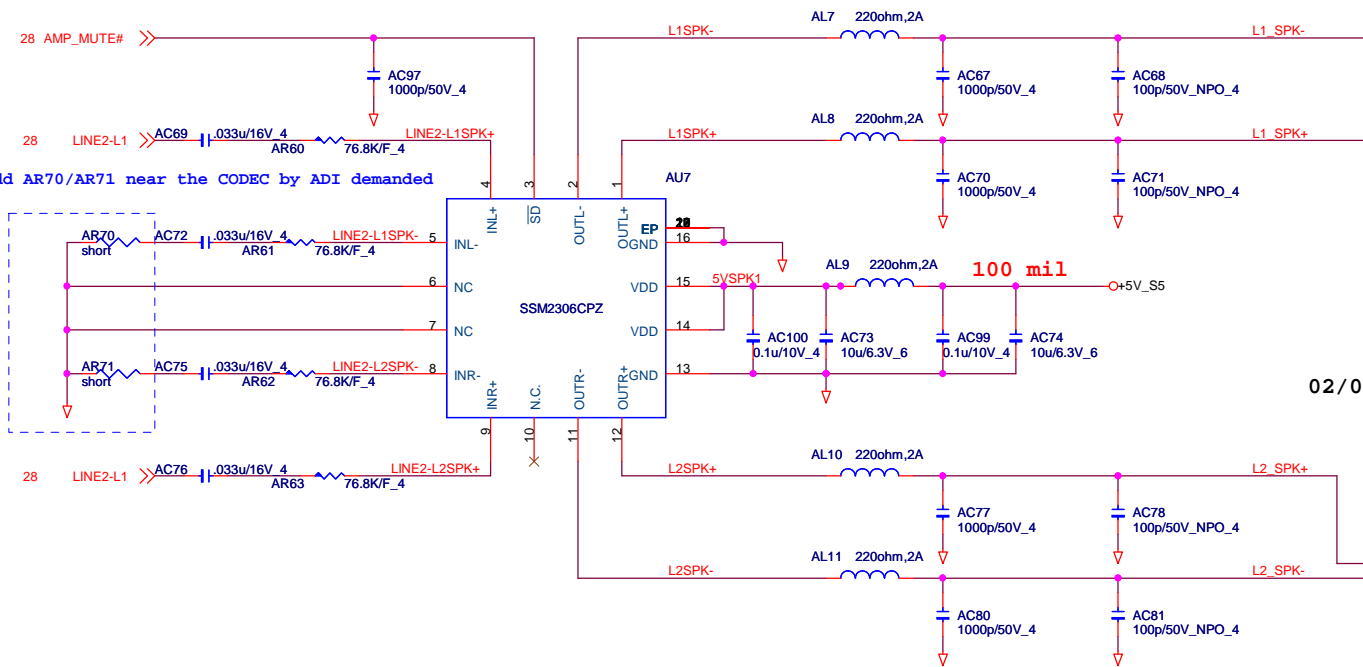
02/05 Change CON2 P/N to DFWF50MR004

01/13 Change the CON5 P.25 Netname from "8028_RST" to "PLTRST#"
01/27 Change the Scalar Board CON5 P.6 from 12V to 3V
02/01 Stuff the D4 for ESD test
02/05 Change the CON5(DP CONN) from right angle type to vertical type (DFHD30MS760)
02/05 Change the CON5(DP CONN) P1,P3,P5 connector +5V power rail for fix scalar power sequence

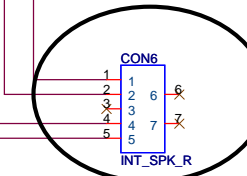


AUDIO AMPLIFIER

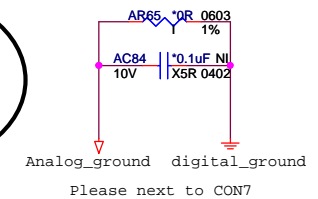
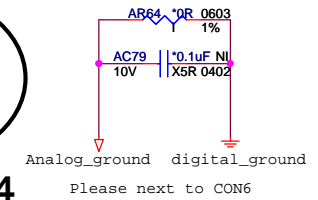
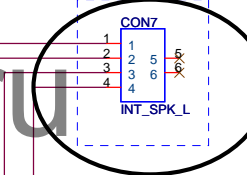
12/22 Add AR70/AR71 near the CODEC by ADI demanded



02/05 Change CON6 from 4PIN to 5PIN (DFHD05MS041)
Change CON7 from 5PIN to 4PIN (DFHD04MR103)



2W X 4



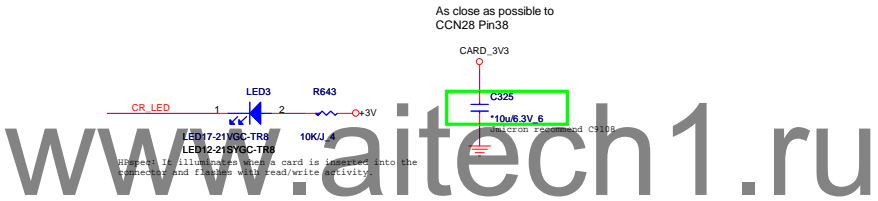
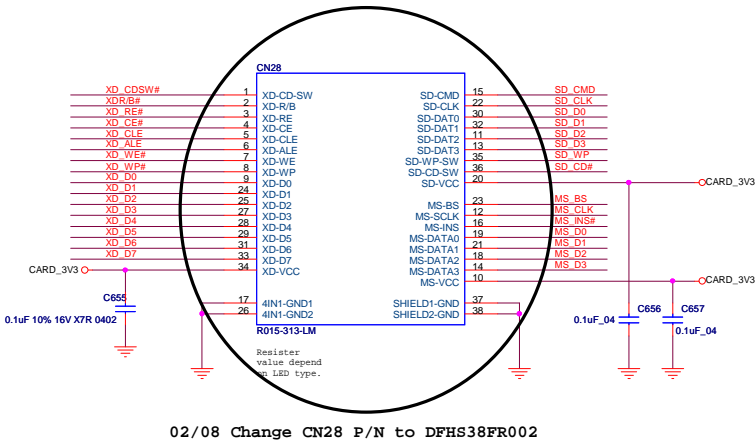
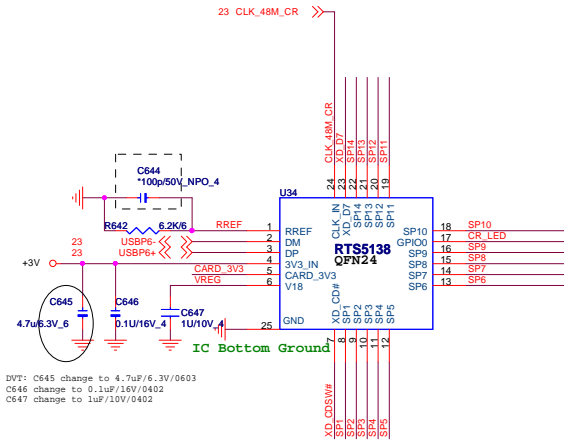
1/28 ME change from 4 to 5pin.
2/5 Change CON6 footprint from 50273-0050n-001-5p-r
to 50273-0050n-001-5p-L



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PROJECT : ZN9

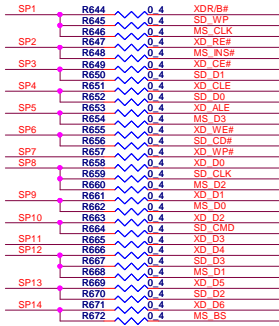
Size	Document Number	Rev
	AMP (SSM2306)	F
Date:	Monday, March 29, 2010	Sheet 29 of 51

6 IN 1 CARD READER



Share Pin

Share Pin	XD	MS	SD
SP1	XD/R/B#	MS_CLK	SD_WP
SP2	XD_RE#	MS_INS#	
SP3	XD_CE#		SD_D1
SP4	XD_CLE	MS_D7	SD_D0
SP5	XD_ALE	MS_D3	SD_D7
SP6	XD_WE#		SD_CD#
SP7	XD_WP	MS_D6	SD_D6
SP8	XD_D0	MS_D2	SD_CLK
SP9	XD_D1	MS_D0	SD_D5
SP10	XD_D2		SD_CMD
SP11	XD_D3	MS_D4	SD_D4
SP12	XD_D4	MS_D1	SD_D3
SP13	XD_D5	MS_D5	SD_D2
SP14	XD_D6	MS_BS	

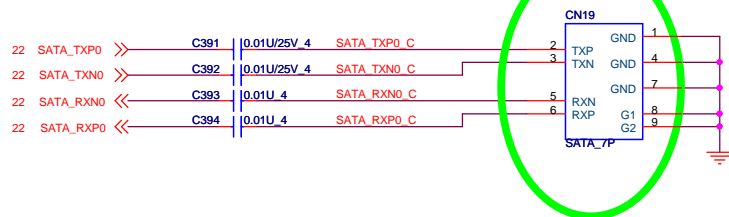


1st 2.5"/3/5" SATA HDD

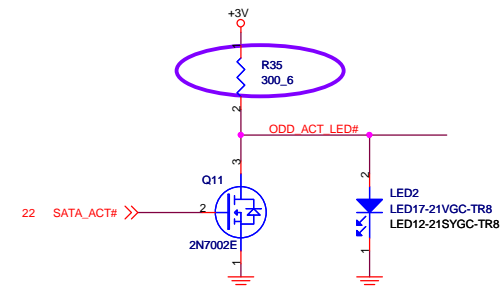
SATA HDD CONNECTOR

From PCH SATA

CAP. Close connect side



SATA HDD CONNECTOR

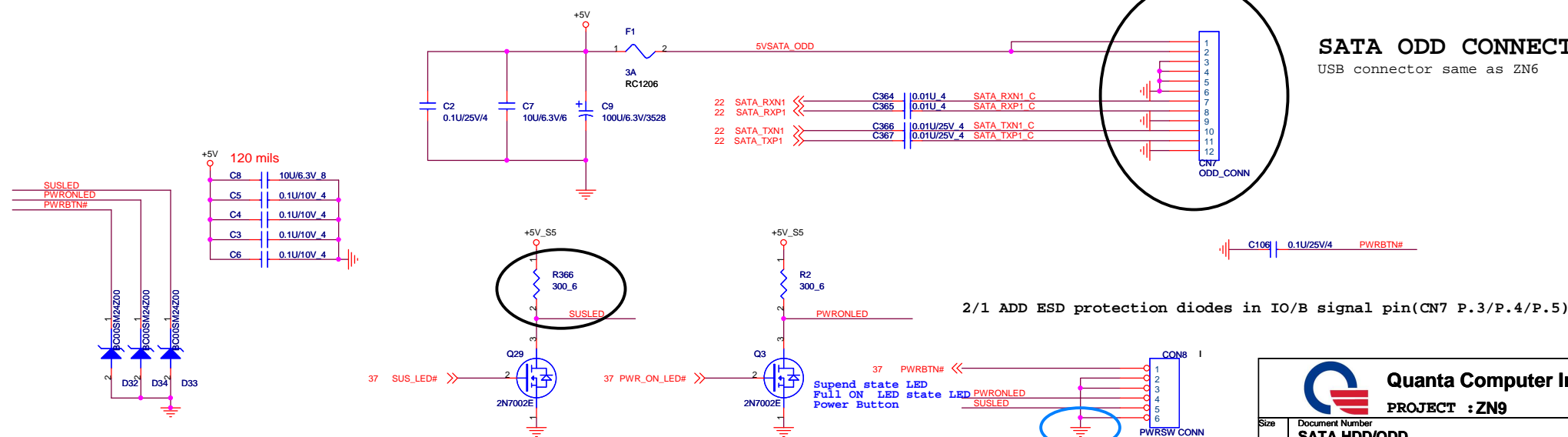


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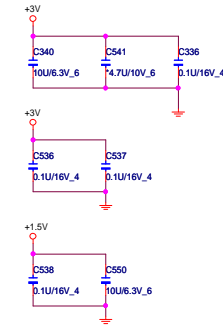
SATA CD-ROM

SATA ODD CONNECTOR

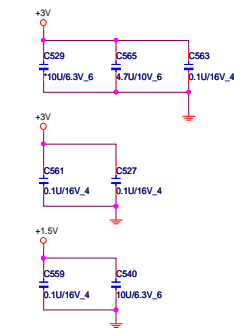
USB connector same as ZN6



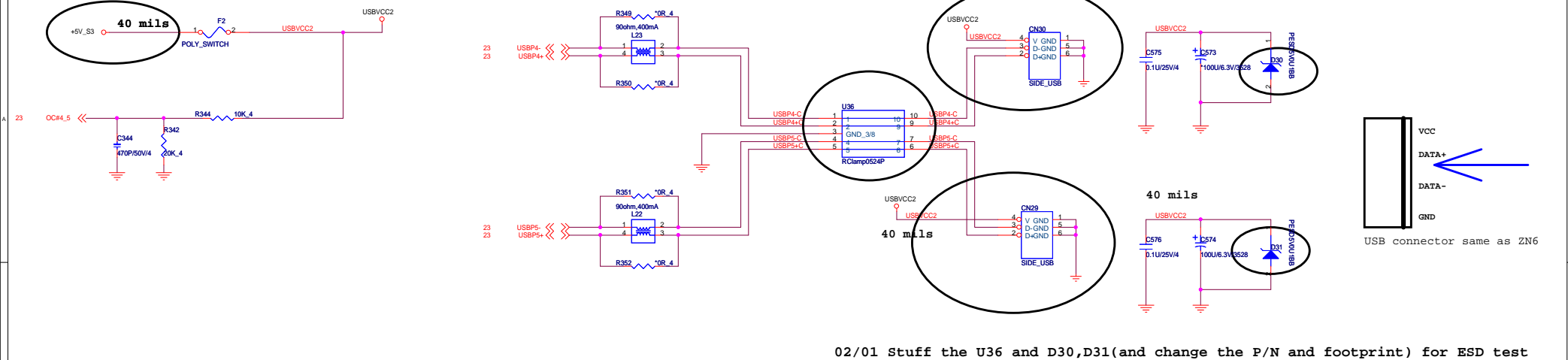
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



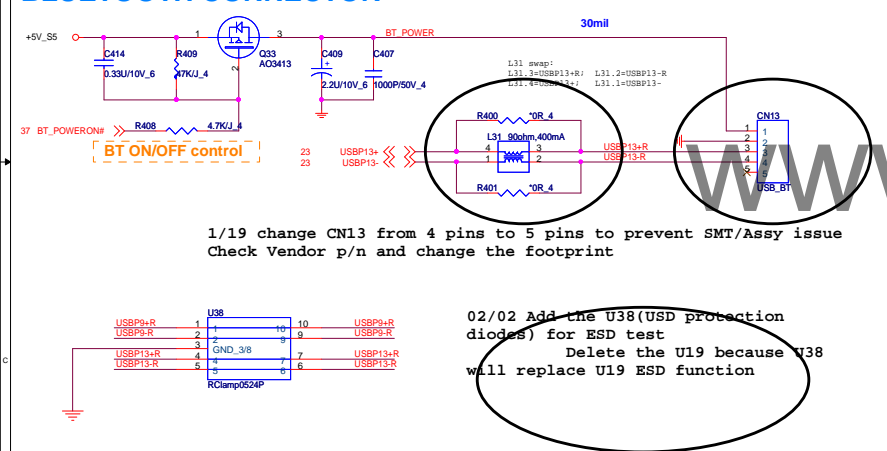
TV



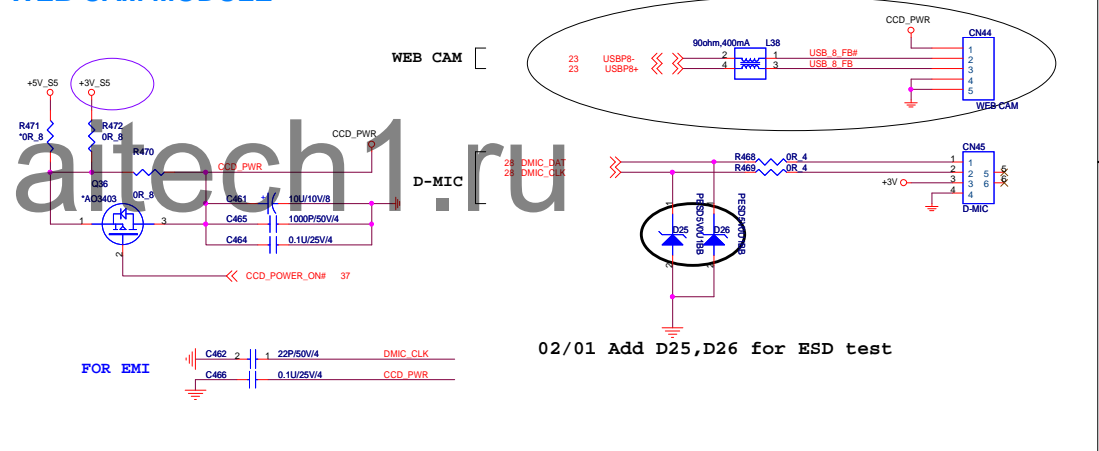
Side USB



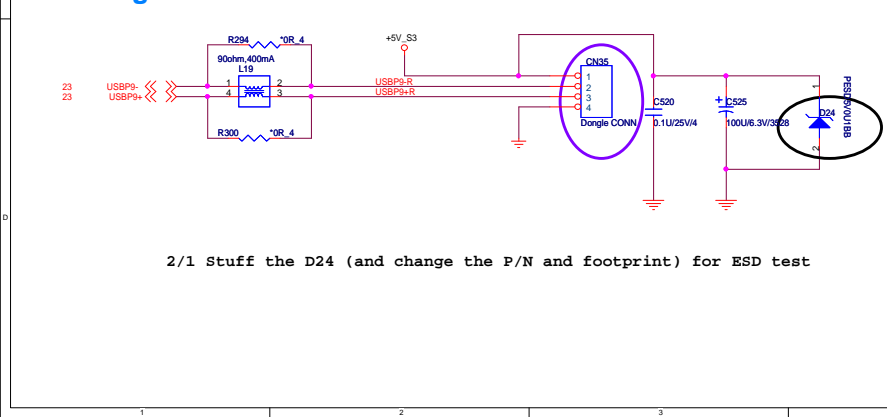
BLUETOOTH CONNECTOR



WEB CAM MODULE

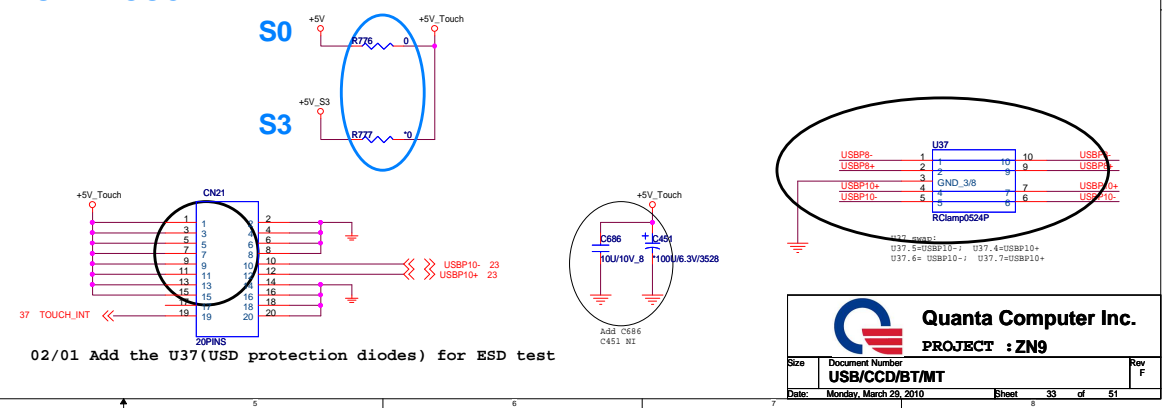


For dongle

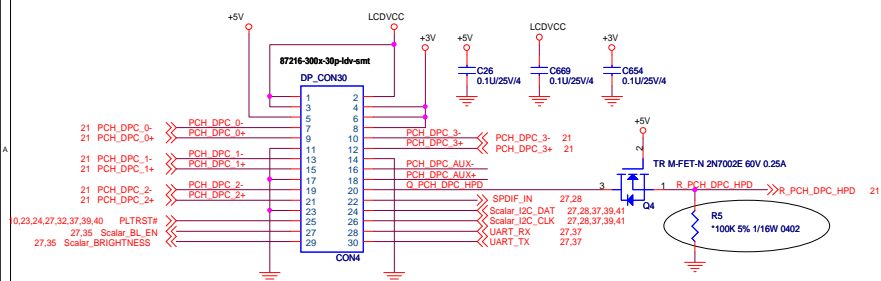


MULTI-TOUCH

HP spec:USB header for touch controller must be able to support 3.0 A.

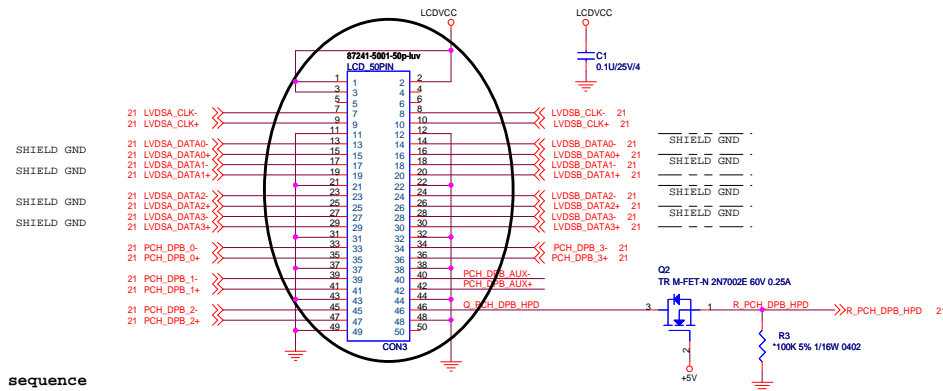


UMA DP CONN for scalar Board



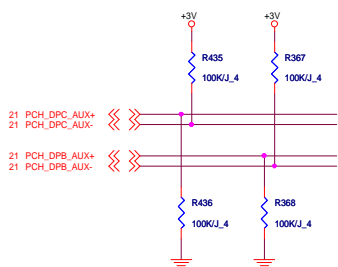
01/13 Change the Netname from "8028_RST" to "PLTRST#"
01/27 Change the Scalar Board CON5 P.6 from 12V to 3V
02/05 Change the CON4(DP CONN) from right angle type to vertical type (DFHD30MS760)
02/05 Change the CON4(DP CONN) P1,P3,P5 connector +5V power rail for fix scalar power sequence

LVDS+DP CONN for UMA



DP I/P and ctrl signal from MB

02/05 Change CON3 P/N to DFWF50MR004

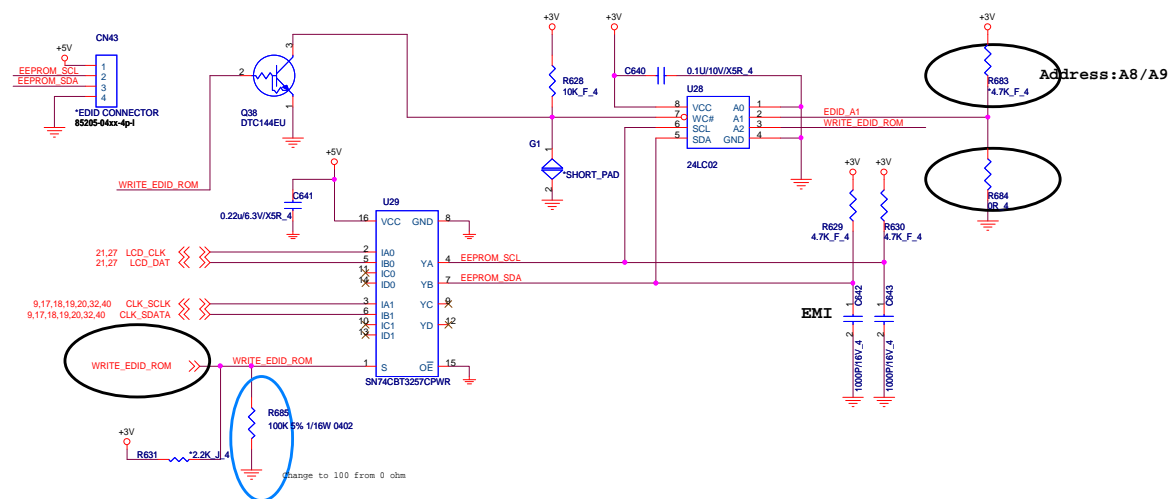


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EEPROM IIC Selection

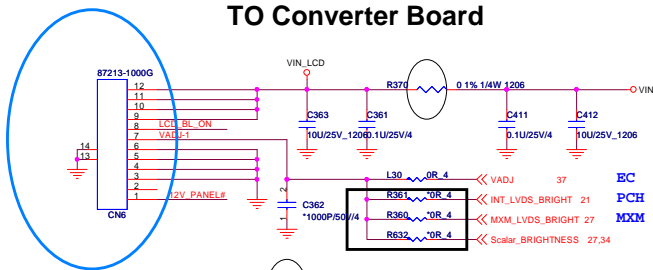
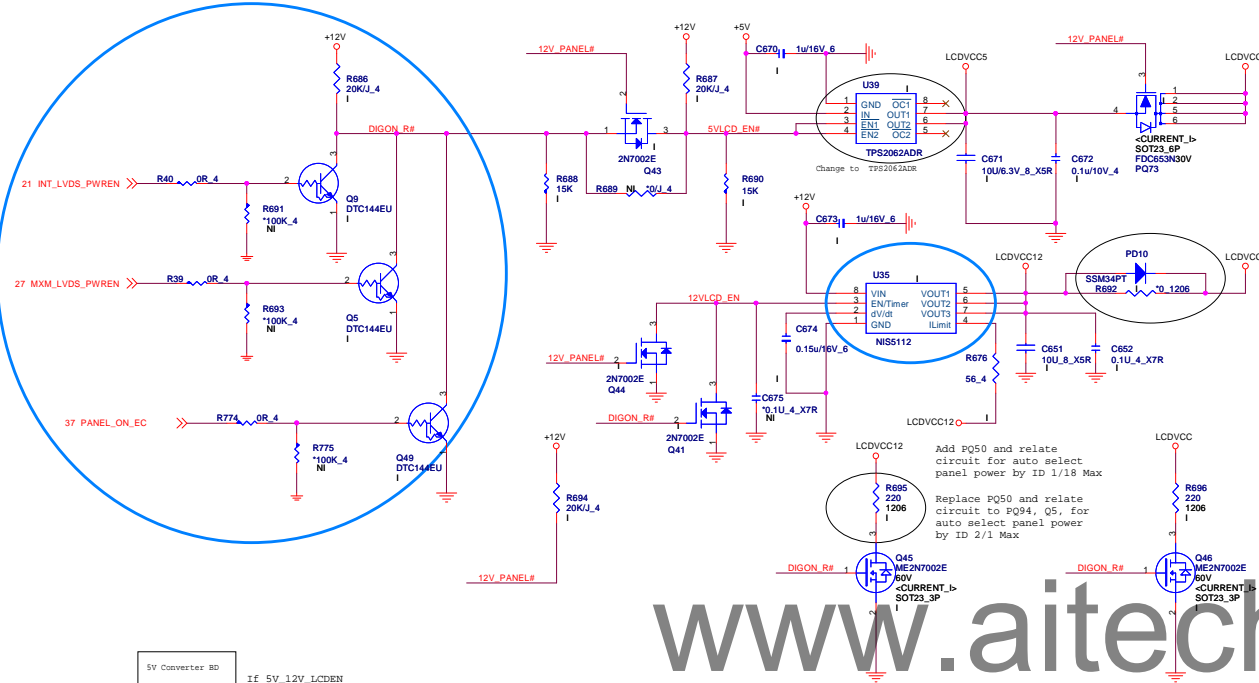
PANEL EDID DATA

02/02 un-stuff the R683 and Stuff the R684



02/02 un-stuff the R631 and Stuff the R685

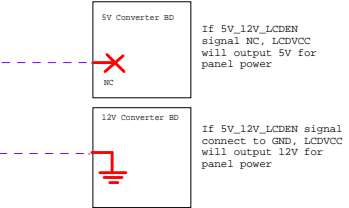
PANEL VCC CONTROL



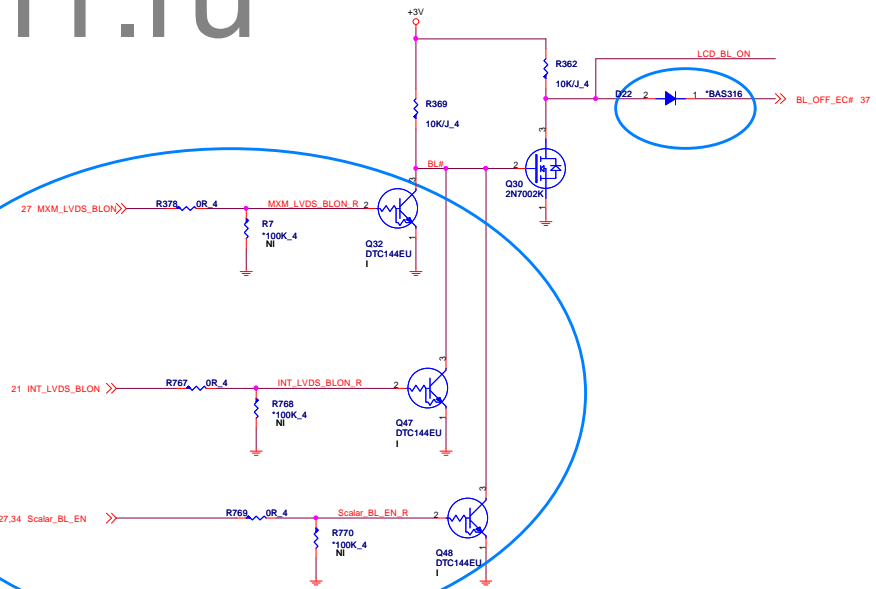
PWM CONTROL

Add on scalar control signal for Cayman ver.
02/05 un-stuff the R360,R361,R632

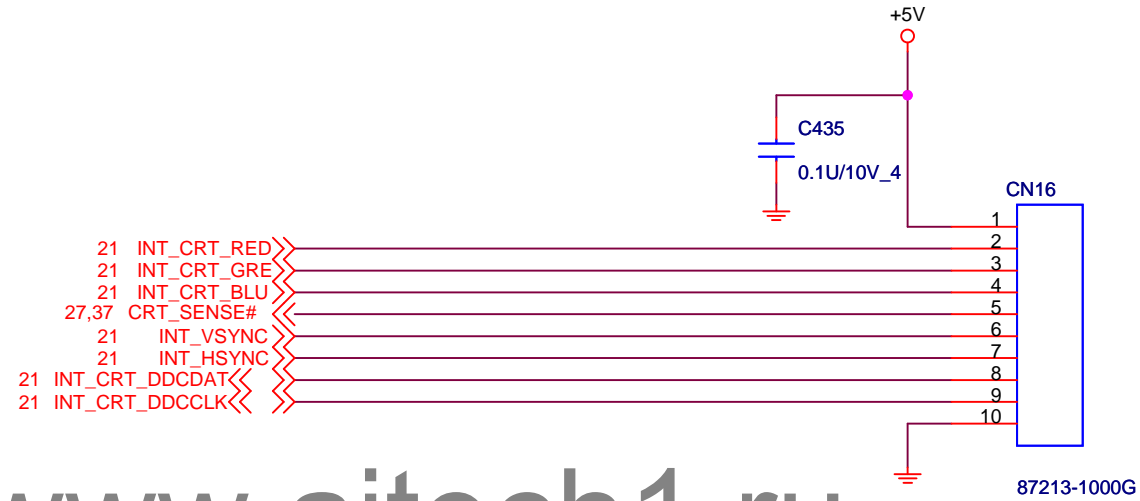
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	Scalar_BL_EN	INT_LVDS_BLON	MXM_LVDS_BLON
Clarkdale - UMA LVDS	0V	3.336V	0V
Clarkdale+MXM -MXM LVDS	0V	0V	3.29V
Lynnfield+MXM - MXM LVDS	0V	0V	3.289V
Clarkdale+MXM + Scalar - Scalar LVDS	3.183V	0V	0V
Lynnfield +MXM + Scalar - Scalar LVDS output	3.177V	0V	0V



CRT for Debug



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PROJECT : ZN9

Size

Document Number

Rev

CRT

F

Date: Monday, March 29, 2010

Sheet 36 of 51



Cancel Braidwood function

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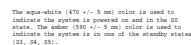
PROJECT : ZN9

Size	Document Number	Rev
	BRAIDWOOD	F
Date:	Monday, March 29, 2010	Sheet 38 of 51

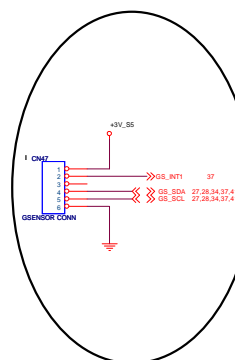
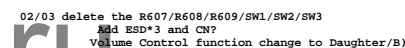
02/01 ADD ESD protection diodes in IO/B signal pin(CONN3 P.1/P.3/P.5/P.7/P.9)



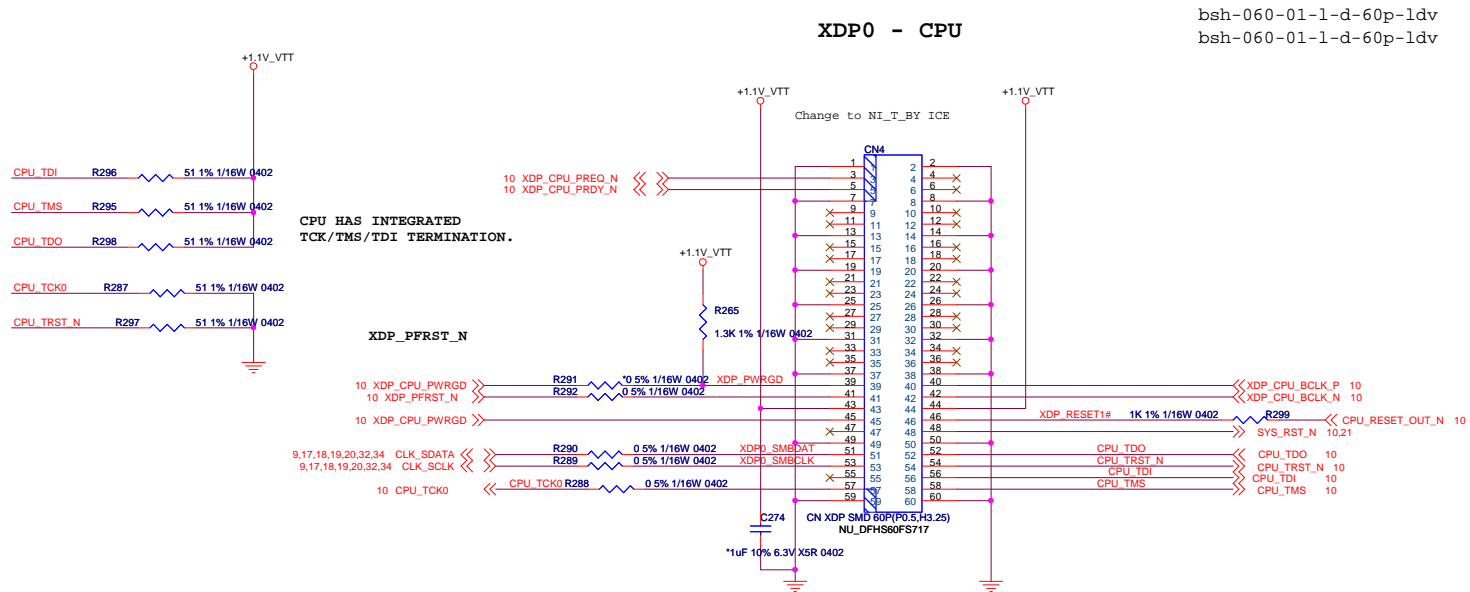
PCIe x1 for
USB3.0 controller



PWRBTN# must pull up to PCU power well

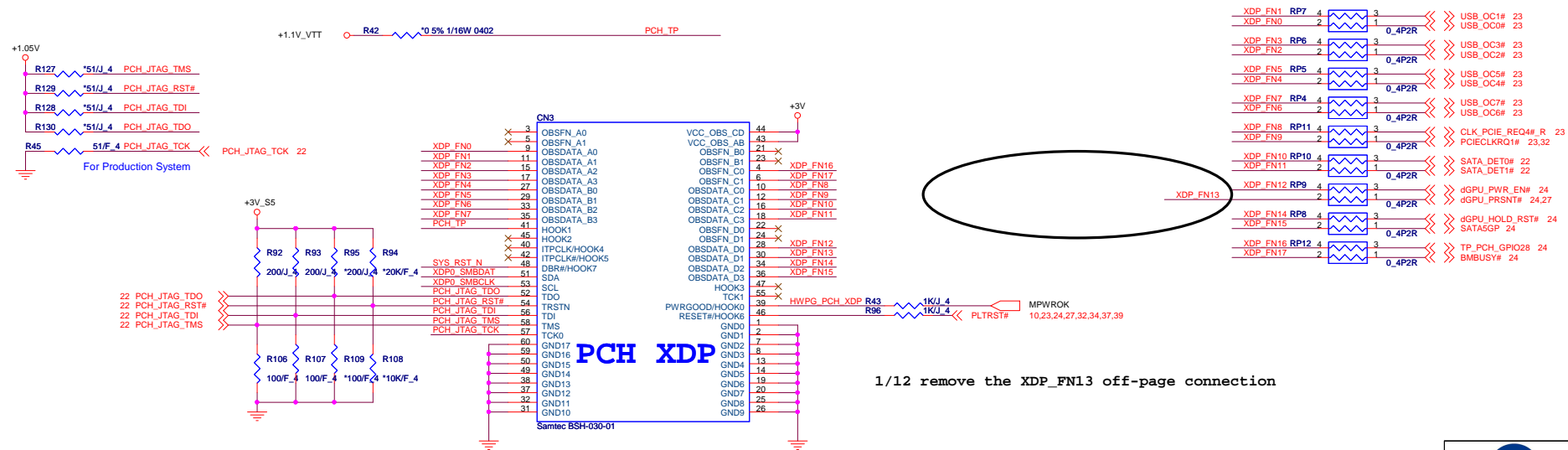


CPU XDP Connector

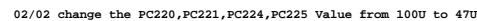


CAD NOTE:
PLACE TDO TERMINATION NEAR XDP CONNECTOR
PLACE TCK/TDI/TMS END TERMINATION NEAR CPU

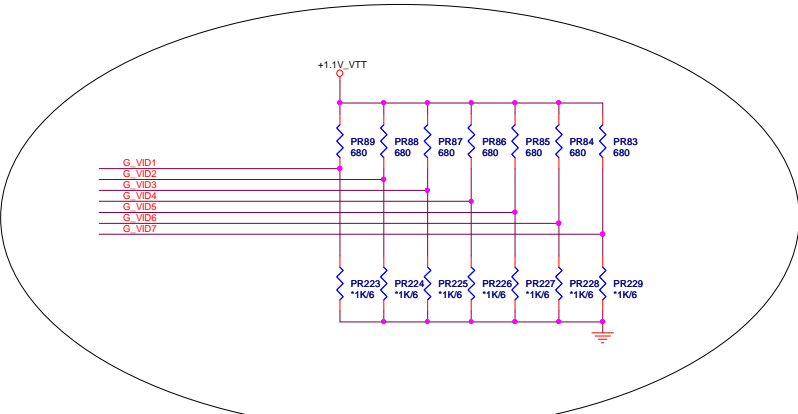
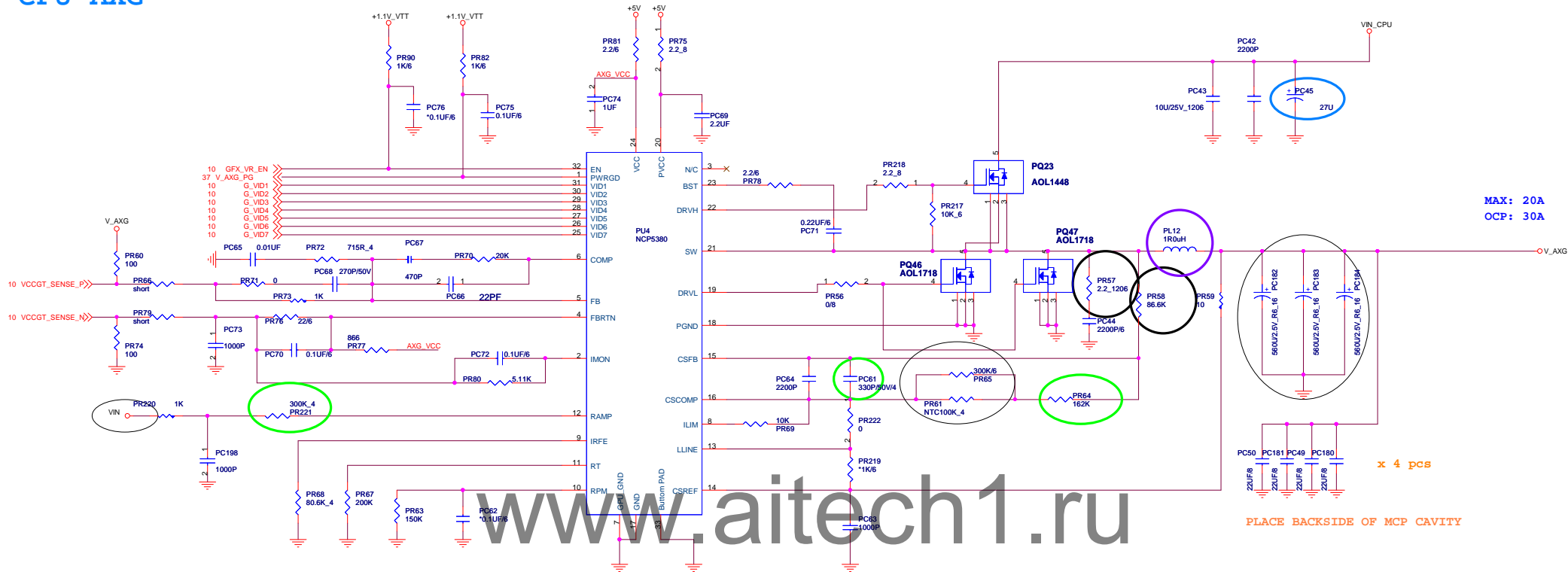
PCH XDP Connector



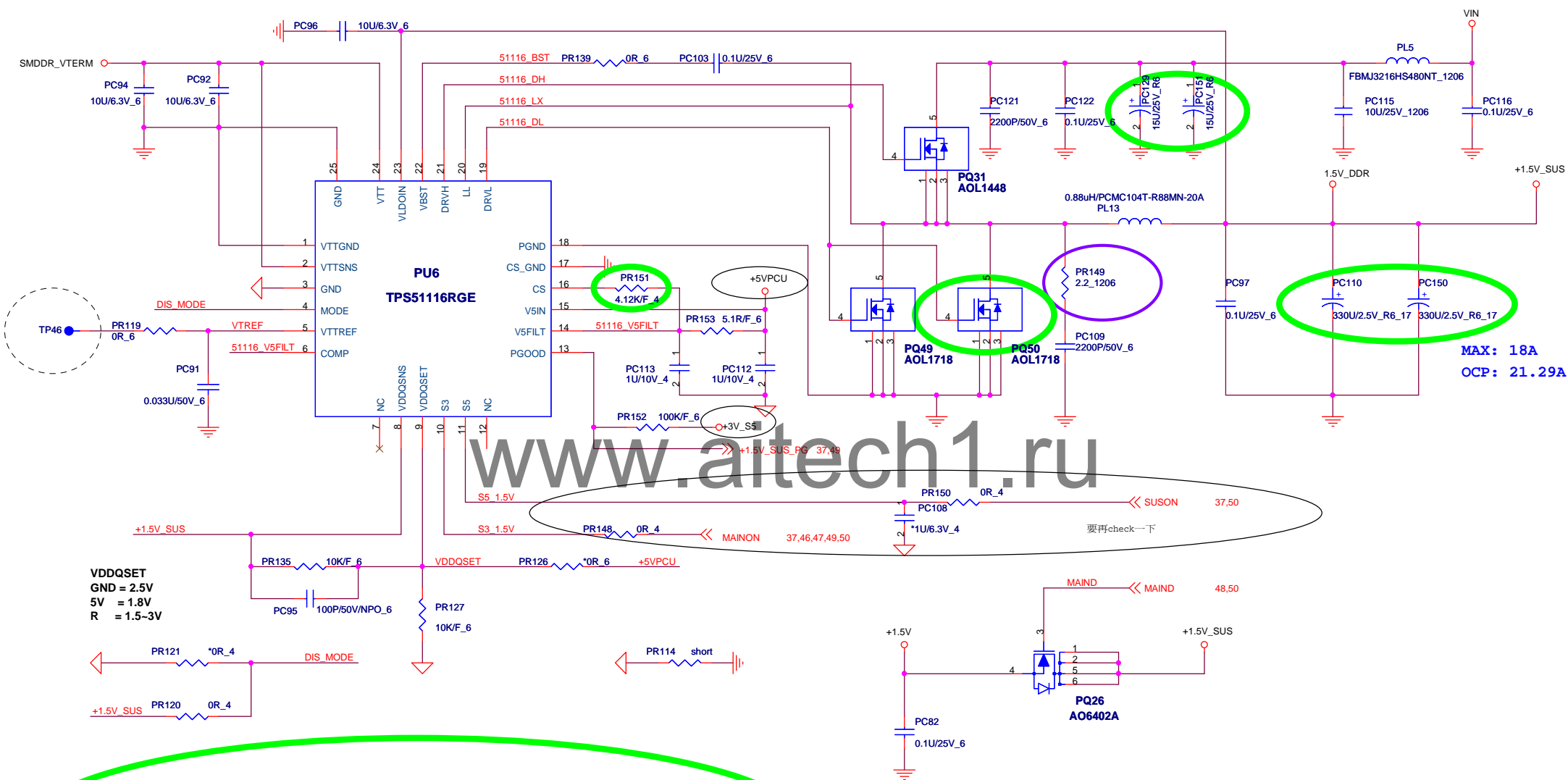
1/12 remove the XDP_FN13 off-page connection



CPU AXG



DDR3 1.5V(TPS51116)

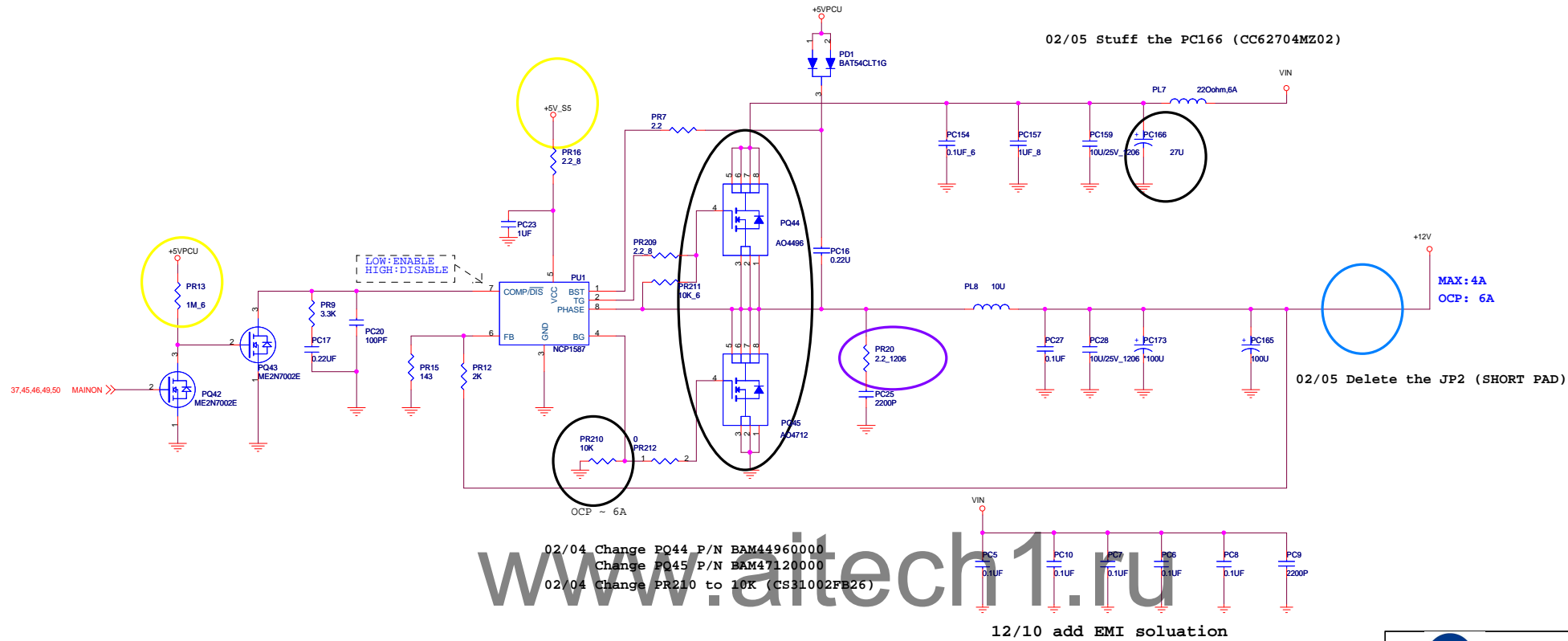


$$\begin{aligned} \text{del_IL} &= (19\text{V} - 1.5\text{V}) * 1.5\text{V} / (0.88\text{u} * 400\text{K} * 19\text{V}) = 3.92\text{A} \\ (10\text{uAxPR26/Rdson}) + \text{del_IL} / 2 &= \text{Iocp} \\ (10\text{uA} * 4.1\text{K} / 2.15\text{m}) + \text{del_IL} / 2 &= 21.029\text{A} \end{aligned}$$

02/02 change the PC222,PC223 Value from 100U to 47U

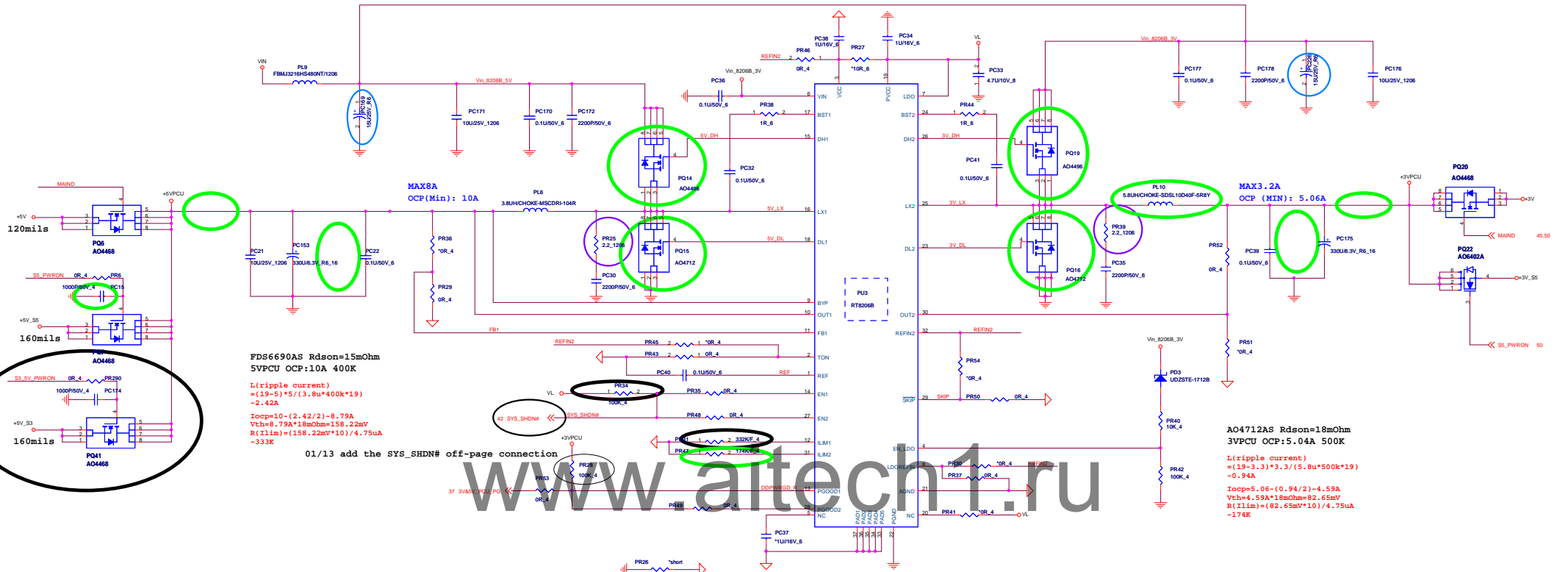


19V to 12V Power CKT



02/04 Change PQ44 P/N BAM44960000
Change PQ45 P/N BAM47120000
02/04 Change PR210 to 10K (CS31002FB26)

3VPCU & 5VPCU
+3V_S5 & +5V_S5
+3V & +5V



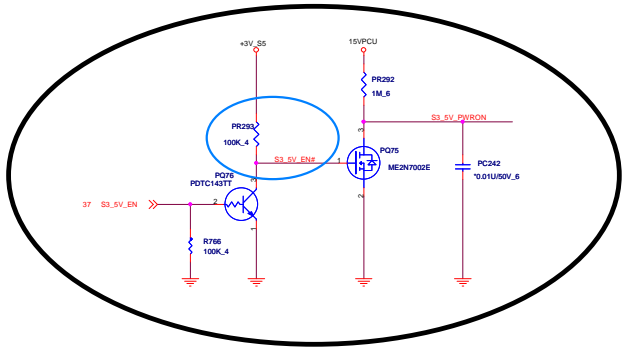
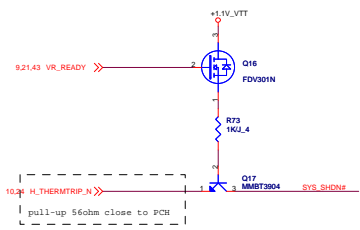
FDS6690AS Rds(on)=15mOhm
5VPCU OCP:10A 400K
 $I_{ripple} = (19-5) \cdot 5 / (3.8u \cdot 400k \cdot 19) \sim 2.42A$
 $I_{ocp} = 10 - (2.42/2) \sim 8.79A$
 $V_{th} = 8.79A \cdot 18mOhm = 158.22mV$
 $R_{(Ilim)} = (158.22mV \cdot 10) / 4.75uA \sim 333K$

AO4712AS Rds(on)=18mOhm
3VPCU OCP:5.04A 500K
 $I_{ripple} = (19-3.3) \cdot 3.3 / (5.8u \cdot 500k \cdot 19) \sim 0.94A$
 $I_{ocp} = 5.06 - (0.94/2) \sim 4.59A$
 $V_{th} = 4.59A \cdot 18mOhm = 82.65mV$
 $R_{(Ilim)} = (82.65mV \cdot 10) / 4.75uA \sim 174K$

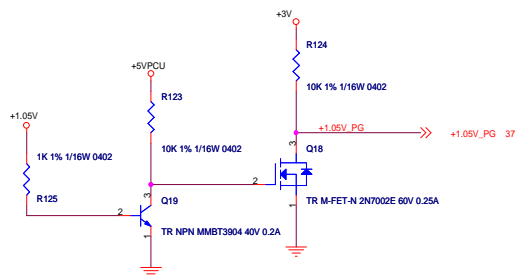
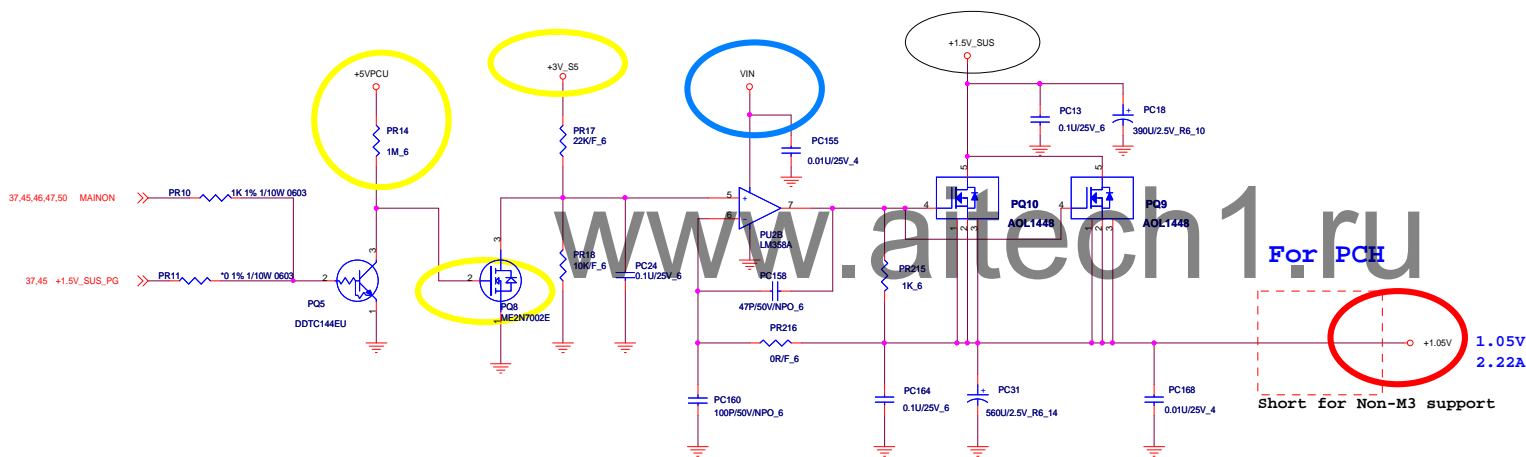
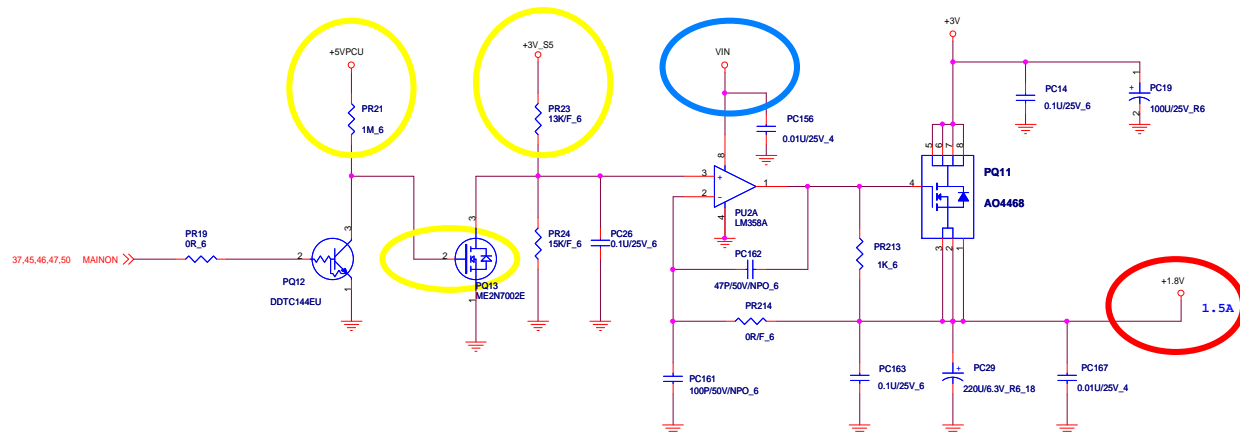
01/13 add the SYS_SHDN# off-page connection

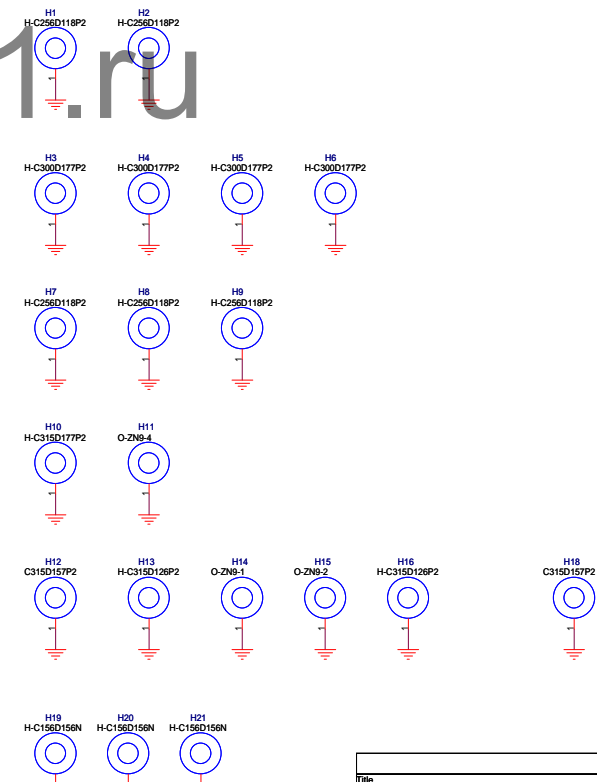
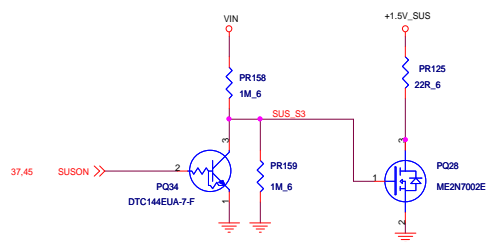
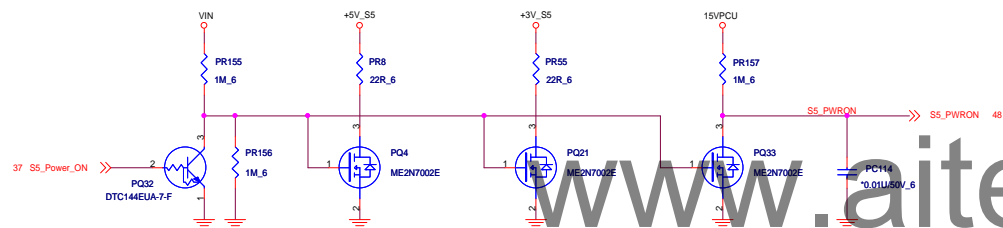
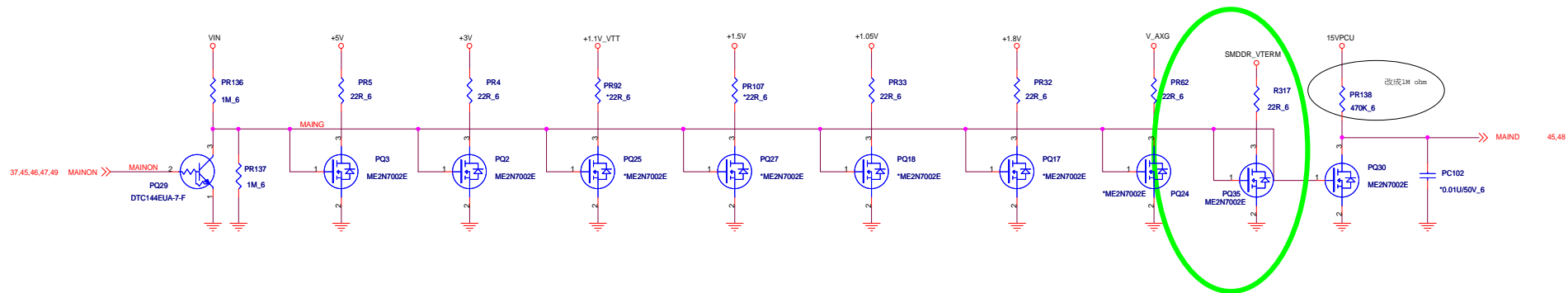
02/01 PR31 change the resistance from 332K to 294K (CS42942FB13)
02/01 PR34 change the resistance from 39K to 100K (CS41002FB28)

Thermaltrip protect



+1.8V & +1.05V





02/05 delete the H22 location

Title		
<Title>		
Size	Document Number	Rev
C	<Doc>	F
Date:	Monday, March 29, 2010	Sheet 50 of 51

Change list			
EVT1.5	1.Remove Vcore output 0 ohm resistor --- R0144,R0145,R0146,R0147 (p.43)		
	2.30V1 signal change pull high to +1.2V_VTT (p.43)		
	3.Remove R0111 (p.45)		
	4.R0115 value change to 10k ohm (p.45)		
	5.1.3V and 0V SWN High/Low side MOSFET change to A051448 --- RQ14,RQ15,RQ16,RQ17 (p.45)		
	6.RJC18R (p.45)		
	7.A061 one C0P (p.45)		
	8.R0121 value change to 10k ohm (p.45)		
	9.R0121 value change to 22k ohm (p.45)		
	10. Change Chime P1A ----> P1B ----> P1C1444411 Postscripta C0000-A05001-1046 P1A ----> 1.530 ----> C0-13000011 Postscripta A05001-1046-1 P117,P118,P119,P121 ----> 0.530 ---->A0-457-000101 PostscriptaA05110300-1046-1p		
	11.C0M change to 3C 3408		
	12.A061 P0701,P0710 Rev 1.3V and 0V power		
	13.R0161A,R0161,R0161,R0161,R0161,R0161 change 120k footprint		
	14.R0161,R0161,R0161,R0161,R0161,R0161 change 120k footprint		
	15. R0121 value change to 4.8k ohm (p.45)		
	16.Control Chime open function --- DEL R555,R556,R556,C09,C40,C07,C23		
	17.C0M1 select signal pull high --- R146		
	18.C07 change to M007004		
	19.R061 speed control change to PWM type		
	EVT2.0	20.Change 1:0 board design (A) 00 pin board to board connector change to 40:20 pin wire to board connector ----> DEL C0001, ADD C0002,C0003 (B) DEL C00 ----> ADD C00A,C00T,C00S (C)	
21.T00A single change to wire to connector			
22.LPC1114 report change connect to wireless miniPCI card			
23.C0M change to vertical type			
24.C0M change to vertical type			
25.DEL SW1 5000 debug connector --- C0020			
26.DEL C154,C158			
27.A061 0-Sensor function			
28. Add 10 pin function for Adapter circuitry			
EVT2.5		1. DEL Backdoor function	
	2. Anular Board connector change to 30pin and add 12V/ 5V0T and 1.7V power		
	3. Vcore power inductor change 0.0 to 0.0-00000000		
	4. Add 000000 for Panel LED		
	5. Add one 3 pin connector for HP Logic light module		
	6. Audio output IC change to A020000000		
	7. Swapphone AMP IC change to T00010002		
	8. Speaker AMP IC change to S00010002		
	9. 24V0,5V00,0V0 0 ohm resistor modified by default		
	10. 0A_C0M1 pull up 0.1 ohm to VTT		
E01	1.R0141 change to 0.2k ohm for fix card reader can't work issue		
	2.D00A data bit swapping for USB trace routing assembly		
E02	3.Change rear I/O connector pinblende and move USB connector close to VGA		
	4.A061 Fan for R02 power		
	5.Modify Mount D1 circuit		
	6.0-MC1 and M0000 separate into two connector (0A-Dan: 5 pin, 0-MC2: 4 pin)		
	7.Change aside 1:0 USB connector for mechanical drawing design		
EVT2.5	E02	8.Change SW13 pin define	
		9.Add 12V/0V switch circuit for panel power (option2 and option4)	

Change list		
F01	1. R20----> R121 stuff the R071 to pull high to +3V; un-stuff the R002	
	2. R20----> R121 Change the C0M1 0.2k Resistor from R0121,20T to V020T20T	
	3. R20----> R121 Change the R002 signal change P-A from 12V power to 3V power	
	4. R20----> R121 Stuff the 04 for R001	
	5. P01,20T ----> Delocate the damage circuit by swap	
	6. 1---->R121 0P segment to change the R02,R02 from C00010 return to C000101	
	7. 1---->R121 0P segment to change the R02,R02 from C00010 return to C000101	
	8. R10----> R121 Add R02 protection diodes in 10k signal pin(CNT P 3.0,4.0,5.0)	
	9. R10----> R121 Stuff the 10k and 10k,10k,10k change the P-A and Footprint1 for R02 test	
	10. R10----> R121 Change R011 from 0 pin to 1 pin to prevent 00T Any issue	
F02	11. R10----> R121 Change R011 from 0 pin to 1 pin to prevent 00T Any issue	
	12. R10----> R121 Change R011 from 0 pin to 1 pin to prevent 00T Any issue	
	13. R10----> R121 Add R02 protection diodes in 10k signal pin(CNT P 3.0,4.0,5.0,7.0,8.0)	
	14. R10----> R121 Add R02 protection diodes in 10k signal pin(CNT P 3.0,4.0,5.0,7.0,8.0)	
	15. R10----> R121 Add R02 protection diodes in 10k signal pin(CNT P 3.0,4.0,5.0,7.0,8.0)	
	16. R10----> R121 Add R02 protection diodes in 10k signal pin(CNT P 3.0,4.0,5.0,7.0,8.0)	
	17. R10----> R121 Add R02 protection diodes in 10k signal pin(CNT P 3.0,4.0,5.0,7.0,8.0)	
	18. R10----> R121 Add R02 protection diodes in 10k signal pin(CNT P 3.0,4.0,5.0,7.0,8.0)	
	19. R10----> R121 Add R02 protection diodes in 10k signal pin(CNT P 3.0,4.0,5.0,7.0,8.0)	
	20. R10----> R121 Add R02 protection diodes in 10k signal pin(CNT P 3.0,4.0,5.0,7.0,8.0)	
F03	40. Change AC LED circuit	
	41. Change AC LED circuit	
	00T: C045 change to 4.7uF 6.3V 0001	
	C046 change to 1.0uF 0.0V 0001	
	C047 change to 1uF 0.0V 0001	
	42. R001	
	43. R001	
	44. R001	
	45. R001	
	46. R001	
F04	00T: C045 change to 4.7uF 6.3V 0001	
	C046 change to 1.0uF 0.0V 0001	
	C047 change to 1uF 0.0V 0001	
	42. R001	
	43. R001	
	44. R001	
	45. R001	
	46. R001	
	47. R001	
	48. R001	
F05	00T: C045 change to 4.7uF 6.3V 0001	
	C046 change to 1.0uF 0.0V 0001	
	C047 change to 1uF 0.0V 0001	
	42. R001	
	43. R001	
	44. R001	
	45. R001	
	46. R001	
	47. R001	
	48. R001	

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